System Architectures for Real Time Power Management

By

Kevin. P. Thomas

A thesis submitted to the University of Bristol in accordance with the requirements of the degree of Doctor of Philosophy in the Faculty of Engineering .

School of Electrical and Electronic Engineering

December 1996.

Abstract

A major characteristic of aircraft evolution is the rapid growth in the electrical and electronic content of each subsequent aircraft generation. The dominant technology used in an aircraft electrical power distribution network to switch power and to protect the aircraft wiring from hazardous electrical faults is the electro-mechanical relay switch and the electro-thermal circuit breaker. Despite the maturity of these devices they do however suffer from a number of problems relating to reliability, accuracy, and limited operational lifetime.

The design, fabrication and testing of a novel Solid State Power Controller (SSPC) is described. The design uses power MOSFET's to provide both the power switching operation of a relay, and the power interruption capability of a circuit breaker. The majority of the control functions required by this device are performed digitally by virtue of a real time program executed on an embedded microcontroller.

A number of methods are derived for characterising existing I^2t wire protection trip response curves. Reproduction of a true I^2t trip response in real time using iterative computational methods is described.

An examination of the semiconductor thermal characteristics was undertaken. The methods adopted for extracting the power semiconductor thermal response involved direct measurement using infrared thermal imaging techniques and simulation using a computer based modelling tool. Knowledge of the semiconductor die temperature is of vital importance in the context of the overall protection strategy. A finite difference calculation performed in real time has been demonstrated as a viable method to predict the operational temperature of the MOSFET power switching devices used in the design.

To my wife Laura and my children Becky and Emma.

Acknowledgements

I would first like to thank my supervisors Dr. Paul Webb and Dr. Stella Mills. I am deeply indebted to them for their continuous support, cheerful encouragement, and the invaluable guidance they have given me throughout the period of this study.

I would also like to thank Professor Michael Rogers for his supervision and guidance during the formative period of this research.

Thanks are also due to Dr. Duncan Grant for his helpful and educational discussions involving the finer points of circuit design and power semiconductors, and to Dr. Gordon Reece for his helpful discussions regarding the intricacies of numerical modelling.

My sincere thanks also extend to my colleagues from the corporate research department of Smiths Industries, especially Dr. David Elliott of the Signal Processing Group who has provided a great deal of stimulating discussion and encouragement through the years, and Dr. Keith Rawlings who has provided continuous support so that I might pursue this field of research. I would also like to thank Jenny and Sue from the Smiths Industries technical library for their tireless assistance in obtaining literature from the most difficult of sources, and the staff of the materials laboratory for their assistance in dissecting so many power devices.

Finally, I would like to thank my wife, Laura, for her support and encouragement, and for shouldering more than her fair share of domestic duties over these last few years.

Author's Declaration

The work described in this thesis has been carried out by the author, K.P. Thomas, unless explicitly stated otherwise in the text.

No portion of the work referred to in this thesis has been submitted in support of an application for another degree or qualification of this or any other university or institution of learning.

K.P. Thomas

12th December 1996.

Table of Contents

Chapter 9

Chapter 10

List of Tables

List of Figures

The Assembled Digitally Controlled Solid State Power Controller

Chapter 1

Introduction and Summary

1.1 Introduction

Until relatively recently, the mechanical switch and the electro-mechanical relay have been dominant as the means of controlling the connection and disconnection of power to an electrical load. Similarly, the thermal fuse and the electro-thermal circuit breaker is the most common means of protecting the power source, feeders and distribution wiring from hazardous current overloads.

As the cost of power semiconductor devices has continuously fallen however, and the electrical performance consistently improved, power semiconductors are now forming the building block of Solid State Power Controllers (SSPC's) which combine the functions of power switching and overload protection within one device.

The advantages these SSPC's have over their electro-mechanical counterparts include factors such as reduced weight, smaller size, faster response time, increased operational lifetime, and the ability to reset previously 'tripped' devices without the need for manual intervention.

Owing to the relatively high cost associated with such devices however, their use has almost exclusively been in the sphere of military aircraft and land vehicles. It is also the case that in these applications there is a continuous demand for higher performance and greater reliability from the electrical system powering mission critical equipment.

The aim of this thesis is to evaluate the control philosophies associated with solid state power protection and to examine new techniques which could improve the performance, functionality and integrity of such devices.

The particular application targeted in this thesis was aircraft electrical power distribution systems; however the techniques and results presented in this thesis are equally applicable to a wide range of industrial applications which require solid state switching and overload protection.

1.2 Summary

The motivation for this research project came from the realisation that the demands placed on aircraft electrical power generation and distribution systems have increased dramatically in recent years. New initiatives in the aircraft industry aimed at reducing weight and operating costs are having a direct impact on the content and structure of the aircraft's power system. Such initiatives include the replacement of hydraulic actuators with all electric solutions [1][2], the downsizing of aircraft electrical generators and the adoption of high voltage (270V) dc power distribution. Similarly the large increase in the electrical and electronic content of modern aircraft means that there is increased focus on maintaining electrical power quality, particularly under fault conditions.

The work detailed in this thesis was directly sponsored by Smiths Industries Aerospace who manufacture power management equipment for a number of modern aircraft. Initial use of some simple commercially available solid state power controllers in a number of the company's products some years ago proved to be highly unsatisfactory. Apart from their high cost, the devices utilised had trip characteristics which were very sensitive to transient overload conditions, and as such, would often nuisance trip when powering loads which had an inrush current demand. More importantly, the devices were often destroyed by subjecting their power output terminal to a short circuit fault.

This experience coupled to the new requirements placed on aircraft power distribution systems was the inspiration for this research project. The main objective was to discover what control functions are necessary to prevent device destruction and what methods could be applied to improve the device performance and to decrease the costs. Initial work focused on the underlying power semiconductor technology, both in terms of determining the desired power semiconductor characteristics, and discovering the operational conditions under which the device can be destroyed. Subsequent work concentrated on examining the control mechanisms required to avoid any such destruction.

As part of this evaluation process it was concluded that numerical techniques in the form of digital algorithms performed on a microprocessor could be applied to such a problem as a method of simplifying the design, increasing the accuracy and providing both additional flexibility and functionality. Two aspects of an SSPC design were of particular interest in adopting this technique. The first aspect was the formulation of an I^2t trip characteristic which models the heating of the wire connecting the SSPC to its electrical load. The second was the task of predicting the die temperature of the series pass power semiconductor device in order that it did not exceed its safe operating temperature. The novel use of numerical techniques to accomplish these tasks has proved to be successful and as a consequence patent application 9514528 has been filed to cover the techniques developed for providing an I^2t trip response curve and patent application 9614590 was filed to cover the die temperature prediction technique. Both these patent applications may be referenced in Appendix 1 and 2 respectively.

The final phase of this research project was to design and construct a solid state power controller which used the protection strategies and the control techniques derived throughout the course of the study. The SSPC developed as a result of this activity was successful in achieving the desired level of integrity and demonstrating the validity of using an integral microprocessing device to perform time critical protection operations. As far as the author is aware no other solid state protection device in existence uses similar techniques.

1.3 Brief Description of Thesis Contents

The thesis is divided into 10 chapters, and their contents are summarised below:

Chapter 1 - Introduction and Summary

Chapter 2 - Fundamentals of Aircraft Power Distribution

This chapter discusses the background to aircraft power distribution. It then proceeds to evaluate the strengths and weaknesses of the electro-mechanical power switching and overload protection technology currently used in aircraft power systems. Finally a review of published literature relating to solid state power control is presented.

Chapter 3 - Review of Power Semiconductor Suitability for a SSPC Application

This chapter provides an assessment of commercially available power semiconductor device types in relation to their suitability in the role of the series pass switching element in a solid state power controller.

Chapter 4 - Assessment of Smart Power Products

This chapter performs an assessment of the suitability and performance of MOSFET devices which have overload protection integrated into the die structure. A number of devices from different manufacturers were tested against the requirements expected of an aircraft SSPC. Results are presented and conclusions drawn.

Chapter 5 - Power MOSFET Destruction Mechanisms

This chapter discusses the operational conditions that will cause damage to a power MOSFET device. It then evaluates various control and protection strategies that need be applied to the MOSFET in order to prevent such destruction.

Chapter 6 - Digital Implementation of Circuit Breaker Characteristics

This chapter discusses the attributes and the broad requirement for an I^2t trip response from any practical SSPC implementation. The problems of trip characterisation are exposed together with a number of solution methods. Finally a comparison of an analogue approach is contrasted with that of a number of digital solutions. Results are presented and conclusions made.

Chapter 7 - Heat Distribution in a Power MOSFET

In this chapter a study is performed relating to semiconductor die heating characteristics under both steady state and transient conditions. The approach taken with this study was to perform die temperature measurements using infrared thermal imaging techniques and to model the problem using a computer simulation tool. These techniques yielded results which were then used to assess the accuracy of a run time temperature estimation algorithm.

Chapter 8 - Power MOSFET Die Temperature Estimation

The problems associated with die temperature measurement using either electrical or physical means in an SSPC are discussed in this chapter. As an alternative, the concept of die temperature estimation is examined and a relative comparison performed of solutions based on both analogue and digital techniques. Finally the chapter presents a derivation of a run time numerical model which predicts die temperature with good accuracy.

Chapter 9 - Practical Implementation of a Digitally Controlled SSPC

This chapter discusses the design and test of a practical SSPC which uses the protection strategies and novel digital techniques detailed throughout the thesis. The first part of the chapter discusses in detail the functional attributes of the SSPC design and important design decisions which were made as part of this activity. The latter part of the chapter presents test results relating to the measured performance of the device.

Chapter 10 - Conclusions and Suggestions for Further Work

This chapter discusses whether the original aims of the project have been met and discusses conclusions that can be drawn from the work. Finally, some suggestions for further work are presented.

Chapter 2

Fundamentals of Aircraft Power Distribution

2.1 Description

The power distribution system is that part of the aircraft responsible for distributing electrical energy from the aircraft power sources (i.e. generators, batteries etc.) to all the installed electrical loads (i.e. fuel pumps, landing lights, cockpit instruments etc.). In addition to this power distribution task, the system also has the responsibility of protecting the aircraft against the occurrence of faults in the electrical system causing a serious hazard such as an electrical fire.

The larger or more complex the aircraft, then generally the larger and more complex the power distribution architecture, this is simply for the reason that on larger aircraft there is generally a greater number of electrical loads requiring power. It is also the case that on larger aircraft there are an increased number of power sources that feed into the distribution system and thus require managing.

Despite this fact, all aircraft power distribution systems rely on the same architecture. Main power cables from the generators and batteries feed into distribution panels installed within the aircraft. These distribution panels contain copper bus bars to which the incoming power feeder cables are attached. On a bus bar individual wire connections are made for each electrical load energised from the bus. Before each individual wire is routed out of the distribution panel en-route to an electrical load or cockpit panel switch that controls the load, it is first passed through an overload protection device such as a circuit breaker or fuse. All protection devices serve the same purpose, in that they

provide a weak link in the electrical wiring that will disconnect the load and associated wiring from the electrical supply if the current demanded by the load exceeds a predetermined threshold (i.e. as in the case of the load developing a fault such as a short circuit). A fuse will physically melt in a controlled manner, thus creating an open circuit and preventing further current flow. Similarly, a circuit breaker will 'trip' on sensing excessive current flow, again creating an open circuit and isolating the fault. A fuse can only be replaced once the wire element has melted and the fault which caused it to melt rectified, whereas a circuit breaker can be manually reset and used many times.

Providing the energy level at which the fuse will melt or circuit breaker trip is smaller than the level at which the wiring will burn, the system will serve to protect against the possibility of an electrical fire which is caused by the wire overheating.

2.2 Current State of the Art

A major characteristic of aircraft evolution is the rapid growth in the electrical and electronic content of each subsequent generation of aircraft. Since the complexity of the power distribution system is closely allied to this growth, many airframe manufacturers have found it more economic to off-load the electrical power management system to external contractors, who, through their systems experience are best positioned to address the complexity issues and develop a working system.

The most recent aircraft developments namely, Lockheed F22, Boeing RAH66, Lockheed C130J, McDonnell Douglas Longbow Apache and Boeing 777, all have electrical power distribution systems developed by external contractors [3][4]. Despite the differing roles for these aircraft, the basic architecture of their power distribution systems are again fundamentally the same. Figure 2.1 provides a much simplified schematic of this basic system architecture:-

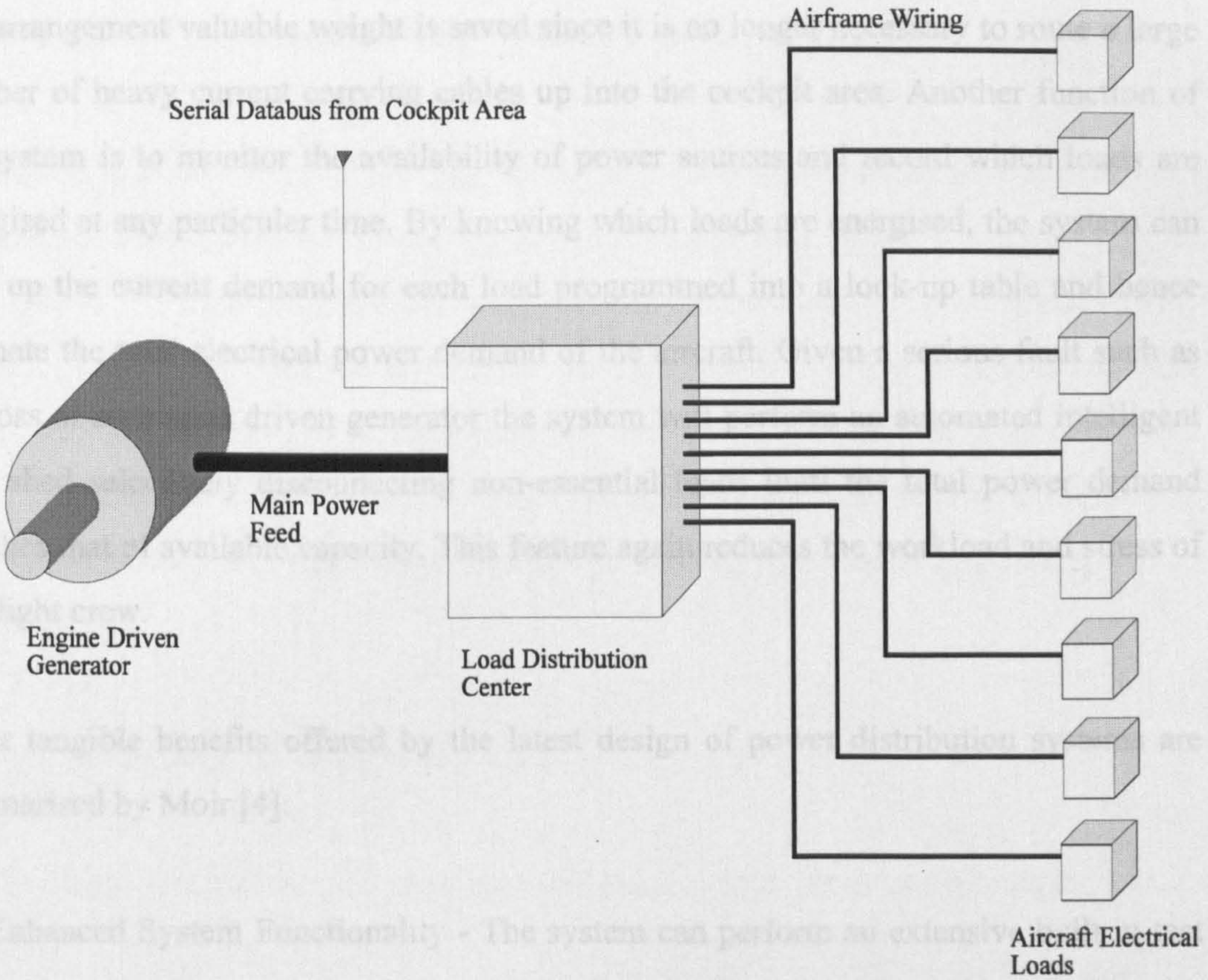


Figure 2.1 - Simplified Schematic Of Power Architecture

From Figure 2.1 it can be seen that main power cables from the generators and batteries are routed into a cabinet known as a 'Load Distribution Centre'. A load distribution centre serves much the same purpose as the distribution panel used in older aircraft, in that the electrical power to the loads is first routed through protection devices housed within the centre.

Where the load centre differs from the older distribution panel is in the fact it contains local intelligence in the form of an embedded microcomputer and can energise and de-energise loads remotely from the aircraft cockpit. In older aircraft if an electrical load could be switched on or off by the flight crew a discrete wire would often have to be routed to the switch in the cockpit area and then onto the load. Load centres can be located closer to a collection of electrical loads and the power switching performed within the cabinet. Switching commands are received via a serial databus (MIL-STD-1553 or ARINC 629) which connects the cockpit control panels to the load centre. With

this arrangement valuable weight is saved since it is no longer necessary to route a large number of heavy current carrying cables up into the cockpit area. Another function of the system is to monitor the availability of power sources and record which loads are energised at any particular time. By knowing which loads are energised, the system can look up the current demand for each load programmed into a look-up table and hence estimate the total electrical power demand of the aircraft. Given a serious fault such as the loss of an engine driven generator the system will perform an automated intelligent load shed selectively disconnecting non-essential loads until the total power demand matches that of available capacity. This feature again reduces the workload and stress of the flight crew.

Other tangible benefits offered by the latest design of power distribution systems are summarised by Moir [4]:

- Enhanced System Functionality - The system can perform an extensive built in test on the aircraft electrical power system aiding the detection of electrical faults prior to takeoff.

- Facilitates More Rapid Airframe Wiring Tests - The system once installed in the aircraft can be used to test the correctness of the subsequent airframe wiring, thus saving a great deal of laborious manual testing by the airframe manufacturer.

- Reduced Volume - Replacement of a large number of discrete wires with a single serial databus connection reduces the volume of the wiring channels. Likewise improved packing techniques mean densities can be maximised.

- Improved Maintainability - The load switching/distribution centres are line replaceable items, likewise many of the individual relays and circuit breakers are also line replaceable. When faults do occur the inclusion of a comprehensive built in test facilitates an accurate identification of a defective module.

2.3 Power Protection and Switching Technology

At present, the dominant technology used for switching electrical power in a load distribution centre and for protecting the airframe wiring from hazardous current overloads is the electro-mechanical relay and the electro-thermal circuit breaker. This technology, together with the techniques associated with it are economical and well understood by designers of aircraft electrical systems. Likewise, the components are well proven and have accumulated millions of operational flight hours. In addition to the maturity issue, the technology also has a number of inherent advantages which include:-

- Positive isolation by virtue of an air gap.

- Handling of ac and dc with equal ease (although ratings are not usually equal).

- The circuit controlling the coil is isolated from the power rail, thus facilitating high side drive configuration.

- High tolerance to over voltage conditions.

- High temperature performance.

2.3.1 Disadvantages of Electro-mechanical Technology

Despite the advantages highlighted in Section 2.3 there are a number of significant disadvantages associated with electro-mechanical technology when considered against the backdrop of industry pressure to both continuously improve power quality and to provide improved levels of protection against electrical faults causing a serious hazard.

These disadvantages can be summarised as follows :-

- The trip curve of a standard thermal circuit breaker has a wide tolerance which often deteriorates further in service (Chapter 6 will examine this topic in detail). This wide trip range makes the systematic co-ordination of protection devices more difficult (i.e. ensuring that the circuit breaker nearest to the fault trips and not an upstream device which will disconnect a larger portion of the distribution network). The wide trip range also prevents the optimisation of cable sizing thus adding to the weight of the distribution wiring.

- For small load currents (i.e. < 5A) an electro-thermal circuit breaker can introduce a significant voltage drop owing to the relatively high resistance of the bi-metal heater element.

- A thermal circuit breaker may take up to 0.8 of a second to trip under short circuit fault conditions. This eventuality can present a significant sag in the voltage of the power rail which is supplying the short circuit current. Sensitive electronic equipment sharing the same supply can often be affected by this break in normal power delivery resulting in system reset conditions which require time to reboot to normal operation.

- The short circuit fault current is only limited by the combined internal resistance of the power source together with the conduction path resistance to the short circuit location. Consequently, fault currents can reach very high levels (i.e. >200A). These large currents mean that when the circuit breaker does eventually trip it often results in the generation of large voltage transients which again can disrupt sensitive electronic equipment.

- Large fault currents usually mean the energy input into the short circuit is also high. This increases the probability of the fault igniting surrounding material, especially where carbon fibre composite materials have been used in the aircraft construction.

- Electromechanical relays suffer from contact bounce, which is a major source of power line transients and electro-magnetic interference.

- Electromechanical devices are prone to ingress problems (i.e. the accumulation of dirt and debris on the switching contacts) and limited mechanical lifetime.

- Electromechanical devices are susceptible to high vibration and shock environments. Under such conditions relay contacts can momentarily open thus interrupting the flow of current to the load. Likewise circuit breakers can trip as a result of movement on the latch mechanism.

- The coil current required to operate an aircraft relay can be as high as 1.5A for some devices. Coil power demands not only represent a significant source of dissipation but are not easily matched to the digital systems that control them.

- Circuit breakers cannot identify open circuit faults, electrical arcing or high resistance faults which result in a current demand lower than the nominal trip level (e.g. a terminal connection not tightened sufficiently). High impedance faults and arcing can be as equally hazardous as short circuit faults as they can generate sufficient heat to start a fire. Open circuit faults whilst not being an immediate hazard can never the less be a cause of concern since they may only be discovered when the function of the electrical item is required.

- The visual status indication associated with circuit breakers is not compatible with digital monitoring systems. Similarly relays require the use of auxiliary contacts in order to convey status. These contacts indicate the position of the contact but provide no assurance that the device is actually operating.

- Since manual intervention is required to reset a tripped circuit breaker, protection devices need to be easily accessible to either the flight crew or ground based maintenance personnel. As such, it is usual that they are centralised into one

location. The consequence of this is that the overall length of the airframe wiring looms are increased as the protection device is usually located some significant distance from both the electrical load and the power source. This situation has associated cost and weight penalties.

2.3.2 Use of Direct Current Generation Systems

In addition to disadvantages outlined in Section 2.3.1 there are changes taking place in terms of aircraft power requirements and generation which is placing additional constraints on the use of electro-mechanical switching technology.

There is a growing preference amongst the developers of major new aircraft to increase the scope of direct current (dc) power distribution for powering aircraft electrical loads. The Lockheed F22 and Boeing RAH66 Commanche are examples of military aircraft which use a combination of 270V dc and 28V dc. Similarly, Boeing, the manufacturer of the 777 passenger aircraft has opted for 28V dc in preference to the traditional 115v ac supply for powering the cockpit instrumentation and flight control systems [5].

The reason for this expansion of dc power distribution is associated with the rapid increase in the number of electronic loads comprised of high density integrated circuits operating from low voltage (+5 to 15v dc) [6]. In older generation aircraft, power for such circuits was generally derived internally by transformer/ rectifier power supplies fed from the standard 115 VAC, 400Hz three phase power input. More recently solid state switched mode dc to dc converters are used as more efficient means of conditioning low voltage dc power, since the 400Hz transformer part of the internal power supplies could be eliminated. By powering the dc to dc converter directly from a dc supply it is possible to eliminate the rectifier unit also and reduce the size of any smoothing capacitors local to the avionics.

Supplying dc from a engine driven generator results in an overall weight reduction of the generator unit owing to the absence of a constant speed drive and the related control necessary for ensuring a constant frequency output. Improvements in generating system maintainability are intrinsically achieved with the reduction in components and complexity.

Paralleling of power sources to maintain uninterrupted power to flight critical systems is simplified with dc power distribution since only voltage regulation of each source is involved (ac systems also involve frequency synchronisation which is much harder to achieve).

Despite the advantages, distributing dc electrical power has important implications with regard to the traditionally used electromechanical protection and switching technology. When switching dc, relays are susceptible to prolonged arcing across the switching contacts due to the absence of the natural arc quenching "zero crossing" characteristic of an ac current. This arcing causes surface evaporation, pitting and oxidisation and rapidly reduces the life of the relay [7]. Relays do exist which attempt to negate this damaging effect by either using fixed magnets designed to deflect the arc thus assisting it to extinguish or by hermetically sealing the switching contacts in an inert gas or a vacuum, which also helps reduce arcing. Such relays are however many orders of magnitude more expensive than a standard relay and as such this prevents their widespread adoption.

2.4 Solid State Power Switching and Protection

Since the mid 1970's an active field of research has been the use of semiconductors to perform both the power switching operation and in most cases the circuit protection function also. The primary goal of the research is to alleviate the deficiencies of electro-mechanical devices highlighted in section 2.3.1. Another driving factor has been the desire to reduce direct equipment costs and cost of ownership associated with power

management equipment. One important trend connected with power electronics is that whilst the performance of silicon power devices is continuously improving the cost of such devices is falling, whereas the same for passive circuit components (relays and circuit breakers fall into this category) are essentially constant, and in fact, the price is gradually increasing [8].

As a result of this on going research, a number of devices have been developed and are the subject of published literature. The devices mentioned are varied in terms of their application and their level of sophistication. The following provides a brief review and categorisation of the technology.

2.4.1 Solid State Relay

A solid state relay performs the same function as an electro-mechanical relay switch, but without any moving parts. The device can be commanded to open or close remotely by virtue of an externally applied electrical signal. No protection function is associated with a solid state relay and consequently the device will be destroyed if subjected to an excessively high load current. The device internally consists of one or more power semiconductor switches which are wired in series with the electrical load. It also contains a small amount of analogue circuitry tasked with providing isolation for the control signal and to allow the device to operate in a high side drive configuration. Commercially available solid state relays are available with ratings from 1 to 100A. The low current devices generally use power MOSFET's as the switching element [9] whilst the high current high voltage devices make use of either Thyristors or Triacs and can be obtained with maximum ac voltage ratings of 1200V [10].

2.4.2 Simple Static Circuit Breakers

A static circuit breaker again uses either a single or multiple number of power semiconductors to directly replace traditional electro-thermal circuit breakers in applications where fast operating speed or arc free interruption are required. Simple analogue circuitry is used to measure the current supplied to the load and to command the turn off of the series pass semiconductor in the event of an overload. The important aspect to note regarding a simple static circuit breaker is that it makes no active attempt to limit the magnitude of fault current and consequently trip times are governed by the maximum transient current rating of the semiconductor.

Tian and Lentz [11] have presented examples of experimental dc static circuit breakers utilising both Gate Turn Off (GTO) Thyristors and Insulated Gate Bipolar Transistors (IGBT's). These circuit breakers have a network voltage limit of 1000V and 450V respectively, and fault current handling capabilities in the region of 4000A. The authors report successful power interruption at the rated current from both devices and as such present a comparison of the results. Their conclusions are that the GTO solution offers higher current and voltage ratings whilst the IGBT solution offers easier gate drive and faster interruption times. They conclude that cooling of the devices represents a significant problem and at this time they cannot be considered competitive compared with classic electro-mechanical interruption techniques. Similar devices utilising GTO Thyristors have been reported by Douglas [12] and De Palma [13]. These devices have a current rating of 100A and again successful fault interruption is reported. Finally a design making use of the recently introduced MOS Controlled Thyristor (MCT) has been also presented [14]. This design uses two MCT's one acting as the in line power interruption device and the other providing a commutation function in order to prevent the fault current from rising above the level at which the MCT can turn off. This device is quite complicated in its operation but the authors report a fault current of 1000A has been interrupted with this arrangement.

2.4.3 Solid State Power Controller

A solid state power controller (SSPC) is the generic name given to a device which utilises power semiconductors to perform both the power switching operation of a relay and the protection function of a circuit breaker or fuse. Like the solid state relay described in section 2.4.1, a characteristic of these devices is that they can be commanded to open and close remotely by virtue of an externally applied signal. Similarly should they trip as a result of an excessively high load current it is often possible to reset the device by application of a reset signal without having to remove power from the controller. Another characteristic of SSPC's is that they normally provide indication of status (i.e. on, off, tripped) by means of a number of discrete signal connections.

As previously mentioned, the level of complexity associated with the small number of devices that have been the subject of published work is varied.

A device falling into the most elementary category has been presented by Kovacevic [15]. This solution uses a simple analogue integrated circuit to provide a trip characteristic in accordance with the safe operating area of the series pass power metal oxide field effect transistor (MOSFET) used in the design. As such, the time to trip is inversely proportional to the magnitude of the overload current which is measured through a low value series resistor. This scheme relies on a fast response time to ensure the power semiconductor is protected from the excessive power dissipation which can result from a short circuit condition. Although the protection device is discussed in some detail no test results or conclusions relating to its performance are provided by the author. A variation of this simple scheme is presented by Capel [16]. In this implementation the series pass power MOSFET is driven into a linear mode of operation on detection of an overload current. In order to prevent excessive heating in the MOSFET die under such conditions current foldback is implemented i.e. the current is reduced in order to lower the power dissipation in the power MOSFET. In addition to this control mechanism, a diode used as a temperature sensor is mounted in close

vicinity to the MOSFET switching elements. This diode monitors the MOSFET temperature and will increase the severity of the foldback as the MOSFET temperature increases. The authors of this paper present some simulated results together with some limited test data showing the feasibility of the control scheme.

The next category of SSPC's are those which incorporate simple analogue circuitry to provide a current-time trip response which is similar in purpose to the I^2t trip response of thermal circuit breakers (this trip response curve will be examined in detail in chapter 6). This current-time trip response circuitry is designed to trip the device in conditions where the load current is not of the magnitude encountered under a short circuit situation but is never the less abnormally high. The time taken to trip is inversely proportional to the magnitude of the current overload. Sturman [17] has provided details of two devices which have this facility, one device uses a MOSFET as the series pass switching element and the other uses a gate turn off thyristor. Under severe short circuit conditions a fast turn off mechanism will be invoked if the load current exceeds a predefined threshold. A commercially available SSPC conforming to a similar design has been outlined by Friedman [18]. The device again uses power MOSFET's as the series pass switching element and control of the device and status feedback is provided by a TTL compatible interface. Similarly another variant of this SSPC category has been presented by Xiaohua [19]. In this design however, the SSPC may operate in an ac environment by virtue of the series pass power MOSFET being incorporated within a bridge rectifier arrangement. All the authors conclude that the designs are successful and the fast turn off under severe current overload conditions is not only to protect the power semiconductor but is also a desired characteristic of an SSPC.

The next group of SSPC's are those which provide current limiting under fault conditions. This feature aims to eliminate the high currents experienced under short circuit situations together with the associated voltage sag and transient generation as detailed in Section 2.3.1. A device conforming to category has been described by Levins [20] and a similar device has been presented by Fachinetti [21]. In both these devices constant current limiting to a pre-set level has been favoured over a foldback current

limiting approach, as many electrical loads have characteristics that cannot tolerate a foldback protection strategy (i.e. loads which demand a high inrush current may cause the protection device to latch). The disadvantage associated with constant current limiting is that under overload conditions the power dissipated in the semiconductor can be much larger than in the foldback case. The device protects against excessive power dissipation by using a resistor capacitor (RC) time constant to turn the device off after 2ms of current limitation. Alternately, a more complex variation of this scheme is presented by Neveu [22] and uses a thermal sensor mounted directly under the semiconductor die to modulate the RC time constant thus turning off the semiconductor device more rapidly if its temperature is higher.

All three authors report satisfactory results from the SSPC designs in that the devices turned off under short circuit conditions without any components being overly stressed. What is significant with these designs however is that the designers do not consider the 'instant trip' characteristic to be a desirable SSPC feature.

The final category of SSPC devices which have been the subject of published literature are those which implement both fault current limitation and a pseudo I^2t trip curve. Baker [23] presents a 5A rated device which uses Darlington transistors as the series pass switching element. This device also implements an unusual arrangement for limiting the stress on the transistor whilst in current limitation, in that it switches a shunt resistor in parallel with the device in order to share the fault current. The time the device is maintained in current limitation before it is turned off is determined from a simple RC time constant. In addition to this protection feature the device also incorporates analogue circuitry to provide a current-time trip response similar to an I^2t trip profile. The author reports satisfactory operation from the device but no details are provided relating to its performance.

The final device in the review was developed by Texas Instruments [24] A pre-set constant current limit is implemented in the device and a single RC circuit provides the protection from excessive power dissipation. A voltage proportional to the voltage

dropped across the switching element when the device is turned on is used as an input into the RC circuit. If the voltage is large, as would be the case if the device were current limiting into a short circuit, this will cause rapid charging of the capacitor. When the capacitor voltage exceeds a threshold value the switching element is turned off. This arrangement provides a semiconductor protection scheme where the turn off time is inversely proportional to the power dissipated in the die. In addition to this protection feature the device also incorporates analogue circuitry to provide a current-time trip response similar to the I^2t characteristic. Owing to the fact the details of this device were obtained from a filed patent no performance results or conclusions were included. It is interesting to note however Texas Instruments do not produce or support this product.

2.5 Conclusions

One of the findings of the published literature review is that the papers have generally been lacking in detail for all but the most simple devices. This is probably attributable to the fact most of the developments discussed are for space or military applications and have been made by commercial organisations. This point has previously been noted by DePalma [13] who concedes that there is a large amount of secrecy associated with the studies. Despite this, it is still possible to make some important conclusions with the respect to the present state of progress in this field of research:-

- The solid state switching/protection devices examined in the review make use of a variety of power semiconductors as the series pass switching/protection element. These devices include - Bipolar Junction Transistors (BJT), GTO's, IGBT's and MOSFET's. Apart from a brief comparison of the IGBT and GTO by Tian [11], and similarly the MOSFET and Bipolar Transistor by Fachinetti [21], none of the papers address the attributes and relative merits of each device with respect to its applicability to the role of a solid state power controller.

- None of the devices examined either claimed, or had the ability to detect or respond to electrical faults which do not result in a current overload, namely: open circuit faults, high impedance faults or arcing of the downstream wire.

- There appears to be no definitive consensus on the protection philosophy which should be applied to SSPC's. Some authors attach merit to the speed at which the device can sense an overload and trip [17]. Others imply merit in a delayed current-time trip response [22]. The question remains on what protection strategies are applicable and what are the constraints imposed by the power semiconductor used.

- The scope of the diagnostic/status output is limited to the states: on, off, tripped and fault. No indication is available as to the reason for a trip which could be recorded and would be beneficial to maintenance personnel in identifying the cause of the fault. Likewise no device provides an output signal indicating the current demand of the load. Such information could provide early indication of a future fault or be used in the larger context of a load shed algorithm.

- All the solid state switching and protection devices reviewed have exclusively used analogue techniques to perform all the protection functions. No exploration has been made into the merits digital techniques may have in terms of improving performance, accuracy, reliability or providing more advanced protection strategies more allied to the requirements of the load.

Chapter 3

Review of Power Semiconductor Suitability for an SSPC

3.1 Introduction

A relatively large array of power semiconductor devices exist at present with most device types being commercially available from a large number of manufacturers. Each type of power semiconductor has a unique set characteristics together with more general characteristics which are shared with similar devices. It is the intention of this chapter to define the desired characteristics of a power semiconductor when used in the context of the series pass switching element of a SSPC. In this role the device is not only providing the switching operation but is also providing the protective function associated with a circuit breaker. Against these requirements each available device type will be examined and assessed in terms of its advantages, disadvantages and overall suitability for this application.

3.2 Selection Criteria for Solid State Devices.

An ideal switch may be defined as a device having zero resistance when 'on' and infinite resistance when 'off'. Additional parameters associated with a power switch include the maximum on current, the maximum current and voltage that can be interrupted, and the maximum off voltage.

For a semiconductor switch the criteria for selection will include:-

- Conduction losses as low as possible : This will reduce power dissipation in the semiconductor switch when in the on-state. This is of primary importance since power dissipated in the switch serves no useful purpose and creates a drop in the voltage supply to the load. Another benefit of low conduction losses are that any heatsinking arrangement can be minimised, saving weight, volume and cost.

- Breakdown voltage as high as possible : This will reduce the susceptibility of the device to damage which may result from voltage transients induced on the power rail. It also enables the clamping voltage of any transient suppression device to be increased, thus reducing the energy absorption requirements of the device (Chapter 5 discusses this topic in greater depth).

- Leakage current as low as possible : This is an issue connected with safety of aircraft maintenance personnel. It is usual practice to isolate a section of the electrical system whilst it is still powered by manually tripping the circuit breaker feeding the section. This would still be possible with a SSPC solution but the larger the leakage current the greater the risk of electric shock when rail voltages are 100V or greater.

- Simple gate drive : Ideally the signal required to control the 'on/off' state of the semiconductor switch will consume little power. If this is so, the complexity and size of the control circuitry will be reduced.

- Current control : A distinct advantage is if the magnitude of the current conducted through the semiconductor switch is under the direct control of the third terminal (gate drive). This feature will facilitate the linear current limiting under fault conditions discussed in Section 2.4.3.

- Low cost : To be commercially viable the device must compete in terms of cost with traditional electro-magnetic solutions.

- Fast response : A distinct advantage is if the magnitude of the current conducted through the device can be rapidly changed by control of the third terminal. This feature will reduce the time required to respond to a current surge caused by a short circuit fault.

We will see later that some of the above requirements conflict and it is necessary to use a compromise governed by the requirements and working operational environment of the SSPC.

3.3 Power Semiconductor Devices

Excluding power rectifiers, the principal type of power semiconductor device is the three terminal switch, in which current flow between the main terminals is under the control of the third terminal (i.e. providing both turn-on and turn-off capability). The control can be either current or voltage and the device can be either three layer (the transistor family) or four layer (the thyristor family). The following sections provide a brief description and evaluation of the types of modern power semiconductors which are available.

3.3.1 Bipolar Junction Transistor (BJT)

A BJT is a continuously current controlled bipolar (two junction) device. Power versions have been widely used in applications such as motor controllers and inverters; however in recent years they have lost much market share to IGBT's and power MOSFET's [25]. State of the art bipolar switching modules are available with ratings up to 1200V, 800A [8].

A BJT is able to conduct in one direction only, hence a single device may only be used to switch a dc supply. In full conduction a BJT exhibits a saturation voltage drop

(Vce_{sat}) of between 0.5 and 2V depending on the current and voltage rating of the device [26][28]. This conduction drop increases slightly with increased collector current.

When considered as the in line switching element of an SSPC, the BJT has a number of disadvantages which would make its use less than optimal. The largest disadvantage relates to the low current gain of the device, typical current gain (hfe) attainable from power BJT's is in the region of 10 to 40, thus for a 20 Amp switch the controlling current into the base needs to be in the order of 0.5A to 2A. Such relatively large drive requirements multiplied by the number of switches likely in an aircraft power distribution system would effectively mean the requirement for a complicated drive arrangement and significant quantities of power to control the switching device.

Another problem associated with the BJT is its susceptibility to secondary breakdown [8]. The device has a negative temperature coefficient which means the hotter a part of the device gets, the more current it conducts - which in turn makes the part even hotter. If this cycle continues the device eventually destroys itself. As a consequence careful management is needed to avoid this problem. A negative temperature coefficient also complicates the process of paralleling devices to achieve a larger current capability, since without external balancing circuitry BJT's will not share current equally.

3.3.2 Darlington BJT

The Darlington BJT is a variation on the conventional BJT in that its current gain is substantially increased to values typically between 100 and 1000 [26] by driving the base current of the power transistor from another transistor. Although the requirement for the relatively high current base drive is eased, the device still retains the other disadvantages associated with the BJT and has some additional drawbacks in that the device is slower to turn off and the leakage current through the device is increased.

3.3.3 Thyristor

A Thyristor is a current controlled device which can be triggered into conduction by a pulse on its gate. A single device may be used to switch either an ac or dc supply but it will however perform a dc rectification of the ac waveform. Although modern Thyristors are available with ratings up to 4500V, 4000A [27] it has characteristics which are not suited to an SSPC application. The major problem is that once it is triggered into conduction the gate loses control and the device can only be turned off by the forward bias voltage across the device falling to zero. If switching a dc supply the device could never be turned off, thus negating any useful purpose as a switching or protection device. The Thyristor has other unwanted characteristics also, in that it is susceptible to being spurious turned on either by excessive dv/dt across its anode and cathode terminals, or by leakage current caused by a high junction temperature.

3.3.4 Triac

A Triac is essentially an integration of a pair of phase controlled Thyristors connected in inverse-parallel on the same chip. The three terminal device can be triggered into conduction in both positive and negative half cycles of supply voltage by applying positive and negative gate trigger pulses respectively. All the problems associated with the Thyristor are equally applicable to the Triac.

3.3.5 Gate Turn Off Thyristor (GTO)

The Gate Turn-Off Thyristor (GTO), as the name implies, is a Thyristor type device that can be turned on by a positive gate current pulse, but in addition, can be turned off by a negative gate current pulse. State of the art devices are available up to 4500V, 3000A and the voltage drop is between 1.6 and 2.8V depending on device rating [28]. No

continuous control of current magnitude is possible via the gate, only on/off control. Another problem that complicates its use in an SSPC is the fact a GTO has a very poor turn off gain (typically 4 or 5) [8] which means that a device conducting a short circuit current of 500A may need as high as 125A negative gate current pulse to turn the device off. The advent of the power MOSFET and more recently the IGBT, has reduced the rationale for using GTO's in the low to medium power applications, but the GTO remains the dominant device in applications requiring ratings above 500A or 1500V.

3.3.6 Power Metal Oxide Silicon Field Effect Transistor (MOSFET)

A power MOSFET is a unipolar, majority carrier, voltage controlled device. It will only block current flow in one direction, consequently a single MOSFET may only be used to switch a dc supply. The magnitude of the current conducted through the device is under the continuous control of the gate voltage. Since it is a voltage controlled device, the gate impedance is extremely high meaning the device takes virtually no current from the gate drive circuit, thus greatly simplifying the drive arrangements. However, during fast turn-on and turn-off the gate needs a current pulse to charge and discharge, respectively, the effective gate source capacitance. A key parameter of a MOSFET is its on resistance. Unlike a bipolar device which exhibits a saturation voltage drop, the voltage drop across a MOSFET is proportional only to its saturated on resistance (Rds_{on}) and the magnitude of current it is conducting. The device on resistance increases with voltage rating and is often cited as following the law: $Rds_{on} \propto (\text{Device Voltage Rating})^{\alpha}$ where $\alpha = 2.5$ [8], Clemente [29] however, states that the true figure is $\alpha = 1.6$. This makes the device increasingly lossy when used at higher voltages. The n-channel enhancement mode is the most common power MOSFET device since its higher electron mobility translates into a lowering of on resistance. Unlike the BJT the device has a positive temperature coefficient making any secondary breakdown negligible. If localised heating occurs for whatever reason, the increase of resistance in the affected area forces the current distribution within the die to be uniform. It will also assist easy paralleling of large numbers of devices (subject to certain constraints which will be

discussed in Chapter 9) which will in turn reduce the voltage drop across the switching device. Single die devices are available with voltage rating up to 1000V or current ratings to 70A [27][28]. Similarly the value of saturation on resistance (Rds_{on}) may range from 4mΩ in low voltage devices [30] to 2Ω for the high voltage examples [27].

3.3.7 Insulated Gate Bipolar Transistor (IGBT)

An IGBT is a hybrid MOS-gated bipolar transistor that combines the attributes of a MOSFET and a BJT. The device is also known as a Metal Oxide Semiconductor Insulated Gate Transistor (MOSIGT), Conductivity-Modulated FET (COMFET) or Gate Modulated FET (GEMFET). Like the BJT the IGBT can only be used to conduct in one direction and consequently a single device can only switch a dc supply. Like the MOSFET, the IGBT is a voltage controlled device and therefore requires negligible steady state current from the gate drive circuit. Similarly the magnitude of the current conducted through the device is under the continuous control of the gate voltage. The device has a higher current density than both BJT and the power MOSFET and as such needs only 30% die size of a MOSFET with similar current rating [8].

Like the BJT the IGBT presents a Vce_{sat} drop across its terminals when fully turned on. With present day devices this voltage drop generally ranges from 1.2 to 4V depending on the rating of the device. The voltage drop curve with respect to conduction current is slightly negative or flat but becomes positive at high current. Where the IGBT differs from the BJT is that it exhibits a negative temperature coefficient at low current densities ($I < I$ nominal) but a positive coefficient at higher currents ($I > I$ nominal). This means the device does not exhibit the secondary breakdown phenomena associated with BJT's. This aids the process of paralleling devices but measures must still be taken to ensure equal current sharing. Discrete devices are available with voltage ratings of 1700V or current ratings of 75A [30].

3.3.8 MOS-Controlled Thyristor (MCT)

An MCT, as the name indicates, is a thyristor like trigger-into-conduction device that can be turned on or off by a short pulse on the MOS gate. Commercially introduced in 1993 [14] this 600V 75A device offers the lowest conduction drop (1.3V) of any semiconductor of comparable power rating.

The device is again voltage controlled and is turned on by a negative pulse with respect to the device anode and turned off with a positive pulse. This mechanism is more complicated than the simple two voltage levels needed to turn on and off MOSFET's and IGBT's and will thus impact on the complexity of the gate drive circuit. Like the Thyristor no continuous control of current magnitude is possible via the gate, only on/off control. Despite the exceptional conduction drop performance, the MCT does have another significant limitations when considered in SSPC switching and protection application. The device is subject to a maximum turn off current rating (120A for the Harris part). As such, under short circuit conditions the device will have to be turned off before the anode current exceeds this capability; otherwise the device will latch permanently in conduction. Since the time to response could be only a few microseconds any control circuit would have to be accordingly fast.

3.3.9 Static Induction Transistor (SIT)

The SIT is a high power high frequency JFET. It is a normally on device (i.e. a voltage needs to be applied to its gate to turn it off) and has found use in very high frequency applications VHF/UHF and microwave amplifiers. Owing to its relatively high on resistance the device is generally unsuitable for general power applications unless justified by the need for high switching frequencies.

3.3.10 Static Induction Thyristor (SITh)

The SITh is a GTO like on off device made commercially available in 1988 [8]. This device is a normally on device, unlike the GTO, and is more robust against spurious turn on. It does however have the disadvantages in that its conduction drop is higher than a comparable GTO and its turn off current gain is lower (typically 1 to 3).

3.4 Comparison of Component Suitability

From the component descriptions given in section 3.3 the power MOSFET and IGBT are considered to offer the best combination of features, in that these devices are voltage controlled and may be used to control the magnitude of current. In order to assess which of the two devices is most suited to an SSPC application, it is first necessary to examine the voltage and current levels to which the device, or devices, would be subject.

3.4.1 Aircraft Voltage Supplies

Contemporary aircraft electrical generation systems have standardised on three nominal supply voltages [Kramer, MIL-STD-704D], namely:

- 115V ac 3-phase 400Hz
- 28V dc
- 270V dc

The 115V ac supply had previous dominance as the primary distribution voltage used in aircraft systems, this was due in most part to the fact it could easily be transformed for

different uses. For reasons discussed in Chapter 2, dc supplies are gradually displacing the use of ac in aircraft electrical systems. The 28V dc supply evolved from 24V dc automotive systems. In common with automobiles, system voltage was governed by available battery technology. The 270V dc supply is derived from full wave rectification of the 115V ac supply.

Although these are the nominal working voltage levels, the semiconductor device will also have to accommodate transient over-voltages as specified in MIL-STD-704D [31]. The 115V ac supply and the 28V dc supply may be subject to a transient level of 180V and 50V respectively for a duration of up to 20ms. Likewise, the 270V dc supply may have transients of 475V for up to 10ms. Given the relatively long duration of these transients it is this maximum voltage which determines the blocking voltage requirement of the semiconductor switching device.

3.4.2 Aircraft Load Current Requirements

Figure 3.1 shows a chart detailing the electrical protection requirements of a contemporary passenger aircraft [32]. The chart shows the current rating of the installed circuit breakers and the total quantity of each type, indicating the number of electrical loads. This load pattern is similar in military aircraft but the total quantity of installed loads is generally lower [33]. From this information it can be observed the most common rated loads are between 2.5A and 10A. Electrical loads requiring a current in excess of 120A are powered exclusively from the 28V dc supply.

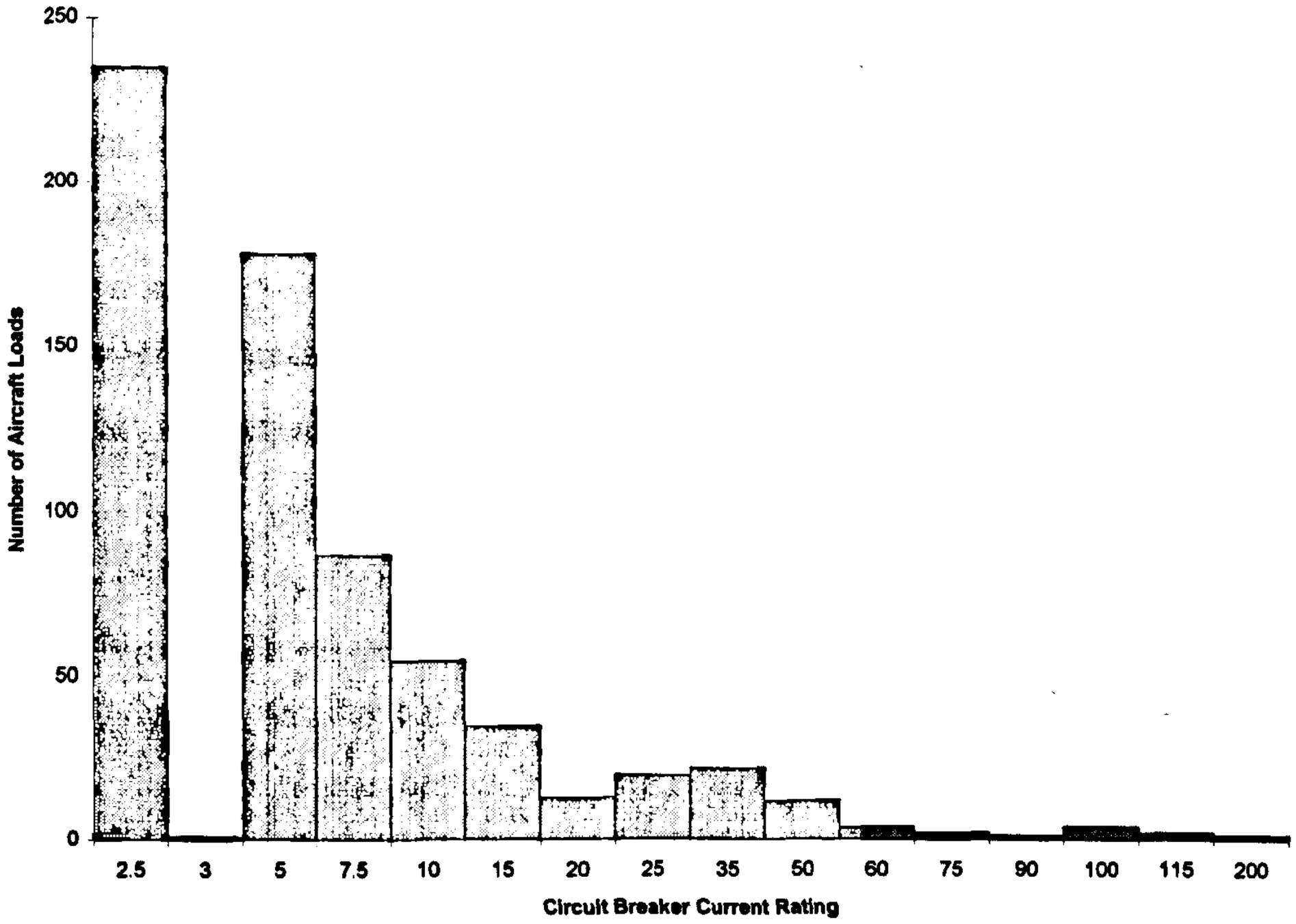


Figure 3.1 Electrical Load Analysis for a Contemporary Passenger Aircraft

3.4.3 Conduction Losses

As previously discussed in Section 3.2 one of the criteria for a solid state switch is that the 'on' state conduction losses should be as small as possible. In the process of examining if the IGBT or the power MOSFET offers the lowest conduction losses it is important to make a fair comparison by ensuring any devices scrutinised have the same current density per unit area of silicon. As such a number of prevailing devices were selected which met this criterion (all have a size 5 die i.e. 6.53mm^2). These devices were:

Power MOSFET's	IRFP054 - 60V Breakdown rating
	IRFP250 - 200V Breakdown rating
	IRFP450 - 500V Breakdown rating
IGBT	IRGPC50S - 600V Breakdown rating

It is evident that only one IGBT is the subject of the comparison. This is because the minimum breakdown voltage rating of IGBT's start at 600V. Consequently, this voltage is sufficiently high to satisfy the all blocking requirements detailed in Section 3.4.1. By contrast, the voltage rating of the three power MOSFET's have been selected to coincide with the voltage requirements, again detailed in 3.4.1. Since the value of Rds_{on} increases with increased voltage rating it is important to match as closely as possible the breakdown voltage of the device with the maximum specified rail voltage.

Figure 3.2 shows a comparison of the voltage drop across the four devices for the current range 0A to 20 A. These graphs were constructed from the values of Vce_{sat} and Rds_{on} provided by the device manufacturer for a case temperature of 25 Degrees Celsius [34][35]. Figure 3.3 again details the voltage drop across the four devices as a function of load current. In these graphs however, the voltage drop for each device type presented relates to operation at an ambient case temperature of 70 Degrees C.

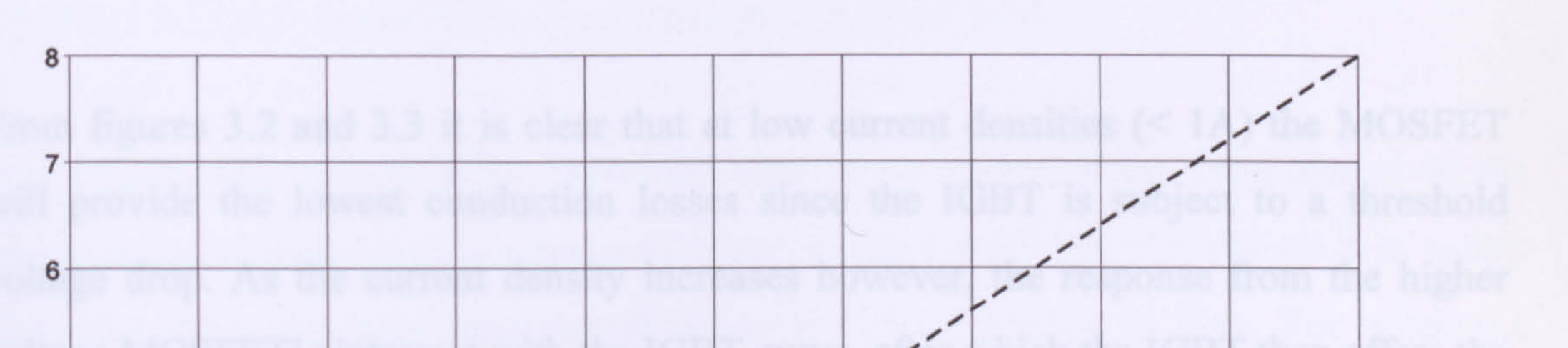


Figure 3.2 Comparison of Device Voltage Drop at 25 Degrees C

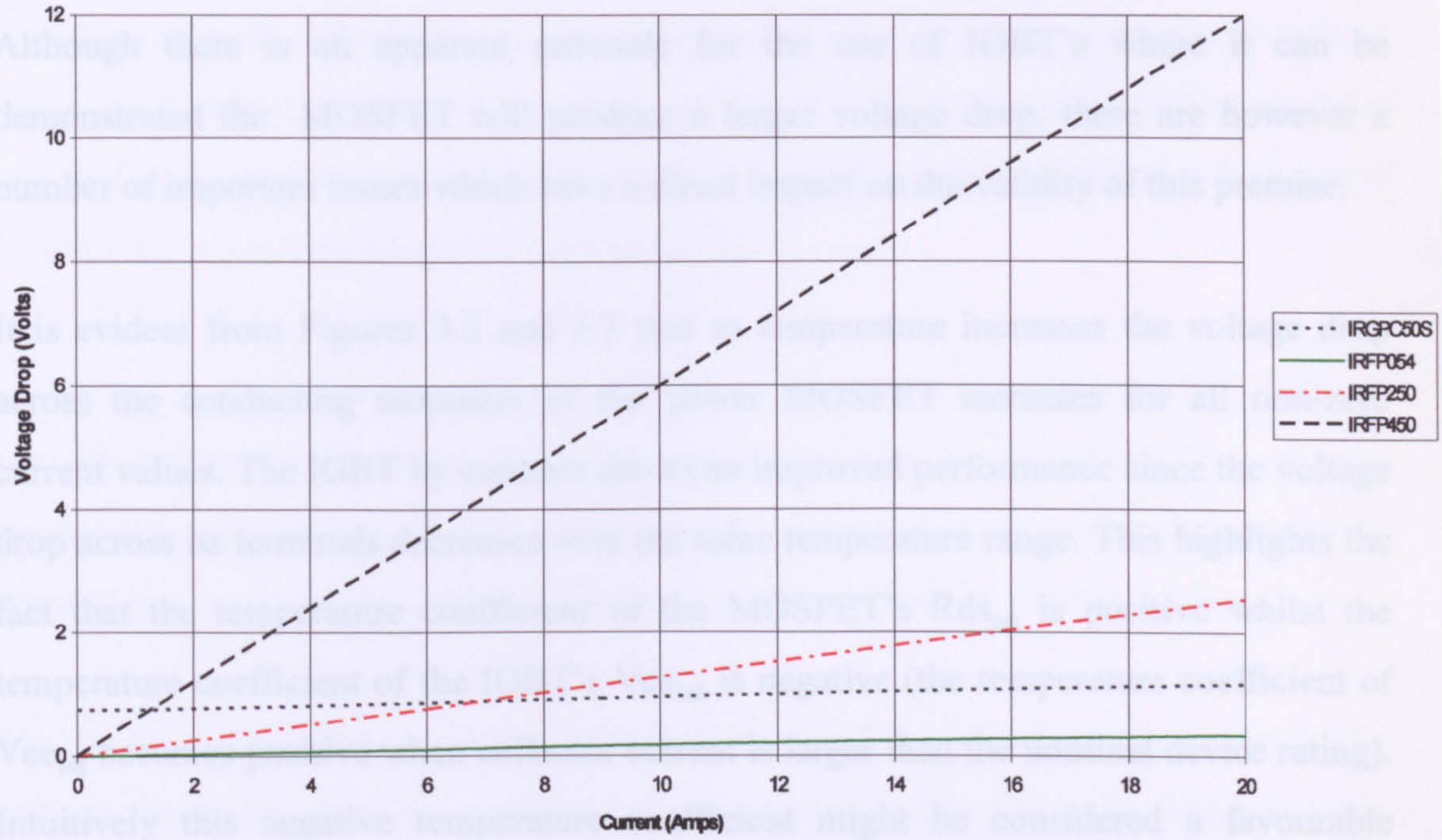


Figure 3.3 Comparison of Device Voltage Drop at 70 Degrees C

From figures 3.2 and 3.3 it is clear that at low current densities (< 1A) the MOSFET will provide the lowest conduction losses since the IGBT is subject to a threshold voltage drop. As the current density increases however, the response from the higher voltage MOSFET's intersect with the IGBT curve, after which the IGBT then offers the better performance. The point at which this intersection happens is dependent on the gradient of the MOSFET curve which itself is proportional to the MOSFET on resistance characteristics. It can thus be inferred that at blocking voltages of 60V or lower the MOSFET offers smaller conduction losses, as the operational voltage requirement increases however, the IGBT increasingly becomes the stronger candidate.

3.5 Discussion

Although there is an apparent rationale for the use of IGBT's where it can be demonstrated the MOSFET will produce a larger voltage drop, there are however a number of important issues which have a direct impact on the validity of this premise.

It is evident from Figures 3.2 and 3.3 that as temperature increases the voltage drop across the conducting terminals of the power MOSFET increases for all non-zero current values. The IGBT by contrast shows an improved performance since the voltage drop across its terminals decreases over the same temperature range. This highlights the fact that the temperature coefficient of the MOSFET's Rds_{on} is positive whilst the temperature coefficient of the IGBT's Vce_{sat} is negative (the temperature coefficient of Vce_{sat} becomes positive when collector current is larger than the nominal device rating). Intuitively this negative temperature coefficient might be considered a favourable characteristic since the temperature of the device will be raised under normal operation by the conduction losses whilst supplying current to the load.

For reasons that will be fully explained later in the thesis, a key requirement of the semiconductor switching element is that it must have sufficient thermal mass to safely dissipate relatively large amounts of power for given periods of time. For economic reasons this thermal mass is best achieved by the paralleling of devices to share the load current. IGBT's will only share current equally whilst in a negative temperature coefficient regime when the values of Vce_{sat} for each device are identical. In practice this parameter is the subject of small variations from device to device [34]. If one paralleled device has a lower Vce_{sat} it will command a larger proportion of the load current. This in turn will result in a higher temperature due to the increased dissipation in the die and will so lead to an even greater imbalance. The problem of successfully operating IGBT's in a parallel configuration has been studied in detail by Letor [36] and Dapkus [37]. Achieving a good current balance requires that all paralleled device are thermally connected by mounting them on the same substrate/heatsink. Balance also requires each device to be operated with a current density approaching the nominal

rating. For reasons that will be explained in Chapter 9, this latter requirement is difficult to guarantee in practice since the required thermal mass will dictate the number of devices needed for a particular implementation. Likewise, the load current may well be below the nominal rating of a single device (Section 3.4.2 indicated loads between 2.5A and 10A as being the most common). In either case the current density per device may be well below the nominal device current rating.

In contrast to the IGBT the positive temperature associated with the MOSFET Rds_{on} is instrumental in balancing the current in paralleled devices. If one MOSFET in a parallel configuration is conducting a larger share of the current, greater resistive heating in the die will increase the value of Rds_{on} for that device so restricting the current flow.

The IGBT voltage drop is of the form $V = V_{th} + rd\ I$ [34] where V_{th} is the device voltage threshold, *rd* is the combined device resistance (device leads, bonding wires etc.) and *I* is the collector current. This implies that the parallel mounting of IGBT's is unable to reduce the voltage drop indefinitely. The voltage drop across a MOSFET is dependent only on the product of the drain current and Rds_{on}. As such if MOSFET's are operated in a parallel configuration, for the same load current the voltage drop across each device will be reduced in accordance with the number of devices paralleled.

Yet another consideration is the switching characteristics associated with each device type. As briefly discussed in Section 3.2, if the device can rapidly control the magnitude of the current passing through it, then under overload conditions the fault current can be quickly limited with the minimum of overshoot. The IGBT, like the BJT is a minority carrier device. The lifetime of the minority carriers in the base of the integral transistor mean that IGBT's suffer from a characteristic 'tail' in the current waveform at turn off. Since the base of this transistor is inaccessible, external circuitry cannot be used to improve the switching time. For this reason IGBT's have a continuous switching performance measured only in a few tens of Kilohertz. The MOSFET by contrast, is a majority carrier device and consequently does not suffer from the same carrier lifetime

problems. For this reason the continuous switching performance of a MOSFET is normally measured in Megahertz.

3.6 Conclusions

This chapter has provided an assessment of commercially available power semiconductor switching devices in relation to their suitability as the series pass switching element in an SSPC implementation. Of all the devices reviewed the power MOSFET and the IGBT possessed the most desirable attributes in that they are voltage controlled thus simplifying the gate drive circuitry and they can operate in a linear region which facilitates fault current limitation.

Despite the fact the IGBT may offer a marginally lower voltage drop at the higher working voltage levels, for the reasons outlined in the discussion section of this chapter the power MOSFET is considered to be the more suitable of the two for use as the series pass switching element in an SSPC.

Chapter 4

Assessment of Smart Power Products

4.1 Introduction

Smart power is the generic name given to a group of products in which a power switching device (predominantly a MOSFET) has been combined with low voltage sensing and control logic on the same die. Early experimental devices used a reverse biased PN junctions to isolate different sections of the circuit from each other [38]. Later devices use either a SIMOX process (using a silicon oxide implantation layer to provide an insulator) or the wafer bonding technique (sandwiching an insulator between silicon wafers) [39].

Within the last few years many smart power products have become commercially available from a number of device manufacturers, including: International Rectifier, Philips, Harris and SGS Thompson. In all these products the on chip control logic provides protection from current overloads by turning off the power semiconductor switch on detection of an abnormally high load current. In addition to this function, many devices also include on chip gate drive circuitry to facilitate its use as a high side drive and signal lines indicating the status of the switch i.e. on, off and tripped. Smart power products would appear to offer the advantage that the switching element is intrinsically protected from the destruction induced by current overload conditions. This is one of the primary requirements of the semiconductor switch when used in an SSPC application. Given the availability of the technology, this chapter provides an assessment of the types of device commercially available and determines the overall

suitability of each device type for the series pass switching element in an SSPC implementation.

4.2 Device Types

The method of overload protection employed by smart power devices falls into two categories:

- Current monitoring products: These devices monitor the current flowing through the switching element by virtue of a small shunt resistor fed from a small number of die cells. The measure of current is input into a comparator circuit and if found to exceed a predetermined threshold the power switching element is rapidly turned off. Once the device has tripped as a result of an overcurrent it can only be reset by driving the gate into the off state. An example of a device using this method of control is the International Rectifier IRSF3010 [27]; this device will trip if the current flowing through it exceeds approximately 12A.

- Temperature monitoring products: These devices offer protection from excessive load currents by monitoring the temperature of the die. This strategy centres on the fact that under current overload conditions excessive die heating will occur owing to the increased resistive heating in the die. The temperature sensor employed by such designs is commonly a forward biased diode powered from a constant current source. Such a scheme utilises the temperature coefficient associated with a PN junction in that the forward voltage drop across it changes with temperature to the rate of -2.2 mV / Deg C. If the temperature of the die exceeds 150 degrees C the device will turn off. Similarly when the die cools to below 120 degrees the device will again resume conduction. Examples of a device series using this method of control are the SGS Thompson VN range of smart solid state relays [40] or the Philips TOPFET overload protected MOSFET's.

4.3 Experimental Tests of Smart Power Products

Experimental tests were performed in order to assess the performance and suitability of the protection methods discussed in Section 4.2. A test circuit was constructed as detailed in figure 4.1.

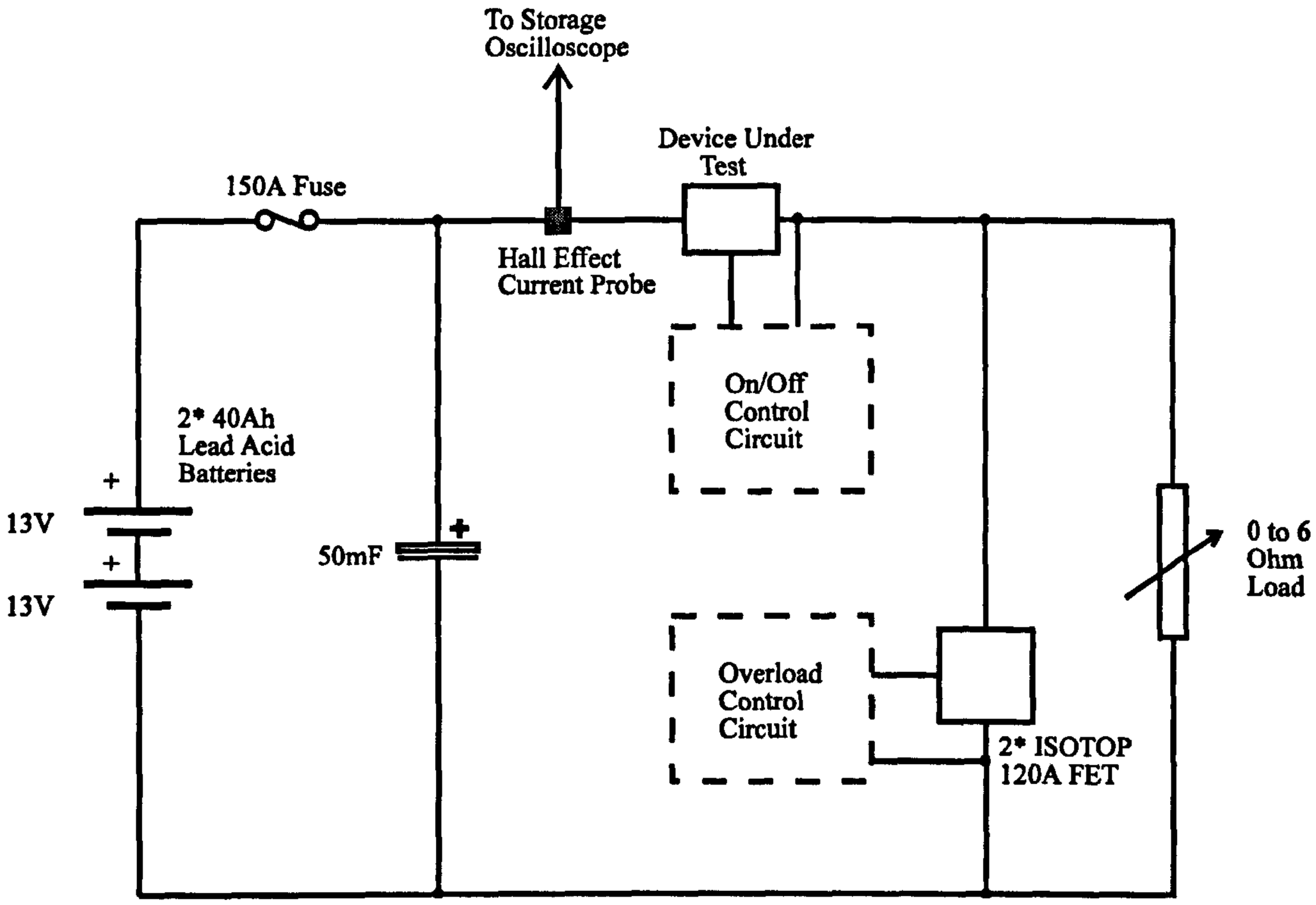


Figure 4.1 Smart Power Device Test Circuit

The test circuit consisted of a power source which had a nominal voltage of 26V (two lead acid batteries wired in series were used for this supply). This configuration could deliver over 200A on a short term basis. For the high current parts of the circuit 380A (0000 AWG) cable was used throughout. Effort was also made to keep wire lengths to a minimum so as to reduce any series resistance and inductance. Current measurements were made using a hall effect current probe and the output waveform could be recorded on a digital storage oscilloscope. The steady state load current could be adjusted by means of a 6Ω 1.5KW rheostat. The device under test was wired in series with this load and on off control was achieved with a simple gate drive circuit. The load could be

shorted out by virtue of two STE25N06 high current (250A) ISOTOP MOSFET modules which were wired in parallel across the rheostat terminals. A control circuit allowed these ISOTOP modules to be turned on for a precise time duration in the range 10μs to 1s (simulating transient current overload faults). Alternatively the ISOTOP modules could be turned on fully for an indefinite period.

4.3.1 Test Results Current Monitoring Device

Figure 4.2 details a typical current trace of the current conducted through an IRSF3010 when it is subjected to a short circuit overload.

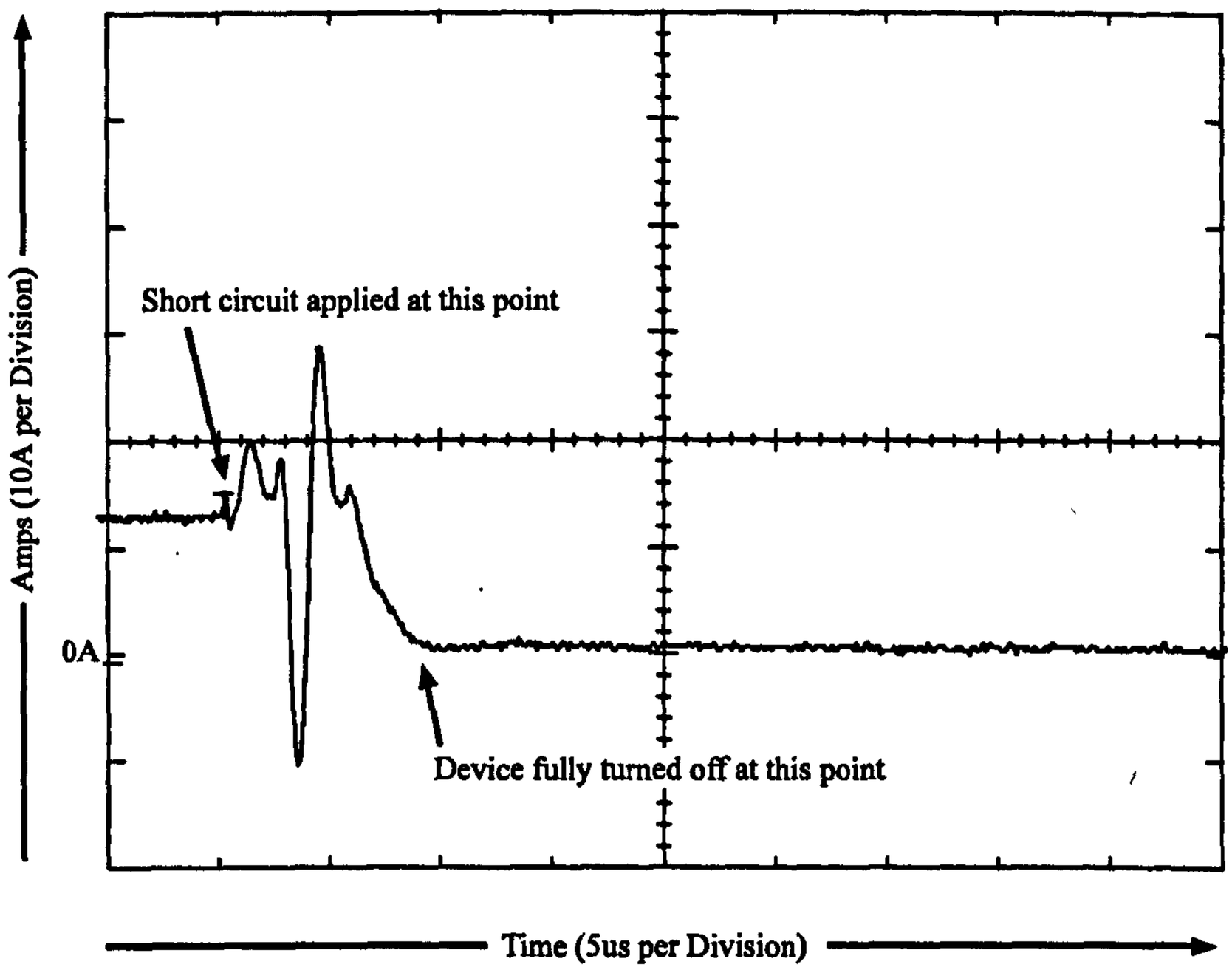


Figure 4.2 IRSF3010 Subjected to a Short Circuit

From Figure 4.2 it can be observed that the steady state load current was set at a maximum value without causing the device to trip off (in this example it was 12.9A). When subjected to the short circuit it can be seen that the device turns off rapidly and circuit current falls to zero within about 8μs. The device latches off on detecting a

current overload and can only be turned back on by first driving the gate to a logic low level and then returning it to a logic high. Alternatively the device may be reset by disconnecting the power supply from the test circuit. A total of 6 devices were tested in this configuration together with other tests such as turning the device on into a short circuit fault. In each case the device isolated the short circuit without incident.

4.3.2 Test Results Temperature Monitoring Device

Figure 4.3 details a trace of load current conducted through a VN20 (28A rating) when subjected to a short circuit overload.

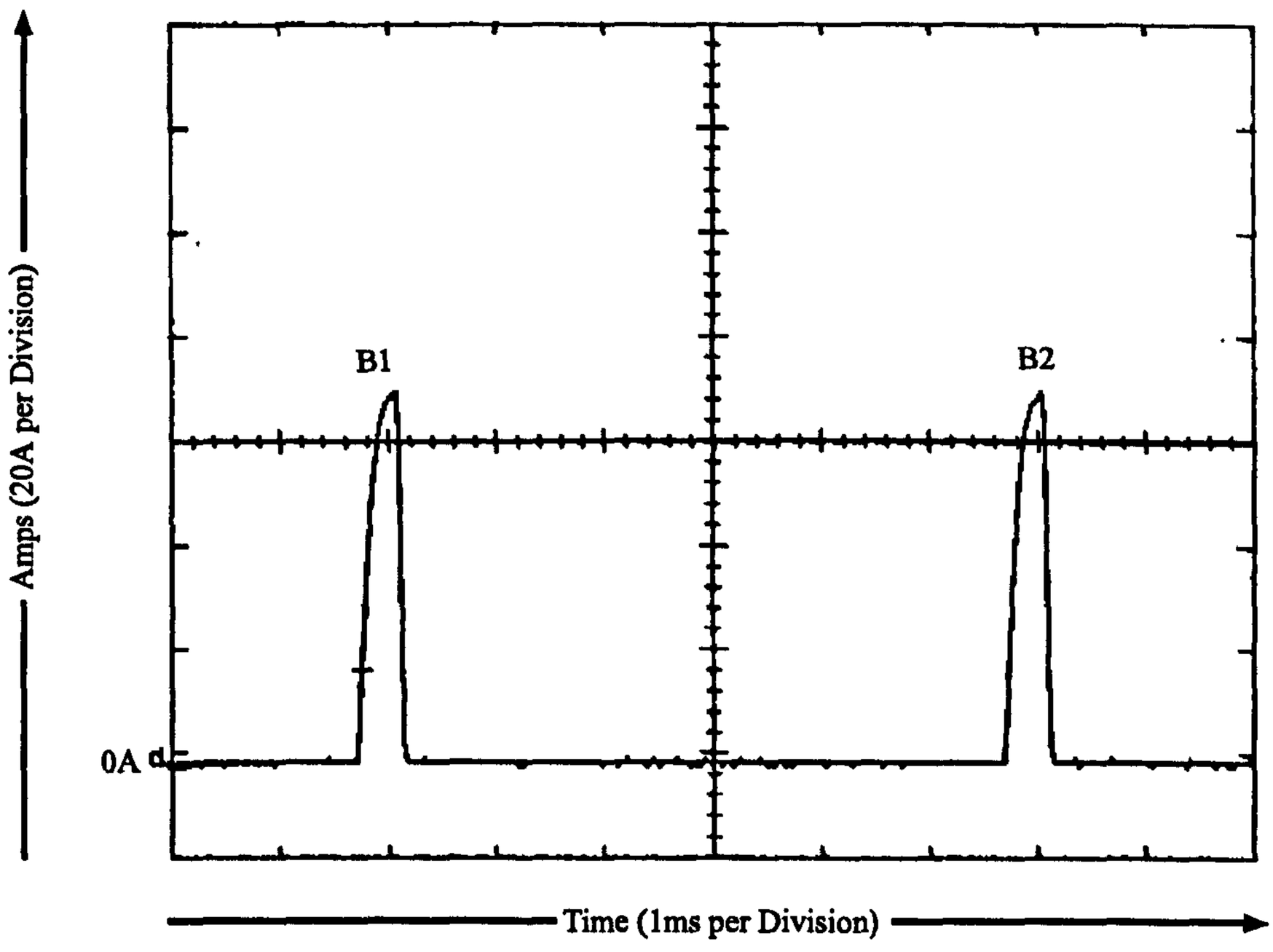


Figure 4.3 VN20 Subjected to a Short Circuit

From Figure 4.3 it can be observed that when subjected to a short circuit the current rises to a peak of 70A (as indicated by point B1), at which point the device turns off as a consequence of the die temperature reaching the maximum temperature threshold of 150

Degrees C. This mechanism produces a spike of current approximately 0.5ms in duration. The device remains off for a further 5.5ms by which time the die temperature has fallen below its threshold of 120 Degrees so it turns on again, this time into the short circuit resulting in the second spike (as indicated by point B2). This overload cycling will continue indefinitely until either the short circuit is removed or the device is turned off. A total of 15 VN20 were tested from three different production batches. Likewise a small number of VN05 (12A rating) and VN16 (5.6A rating) and Philips BUK105-50S (29A rating) devices were also tested in an identical manner. This short circuit test always resulted in the eventual destruction of the device under test. Destruction was relatively instantaneous, but on a few occasions the device contained the short for a few seconds before expiring. Figure 4.4 details a typical current trace of device destruction.

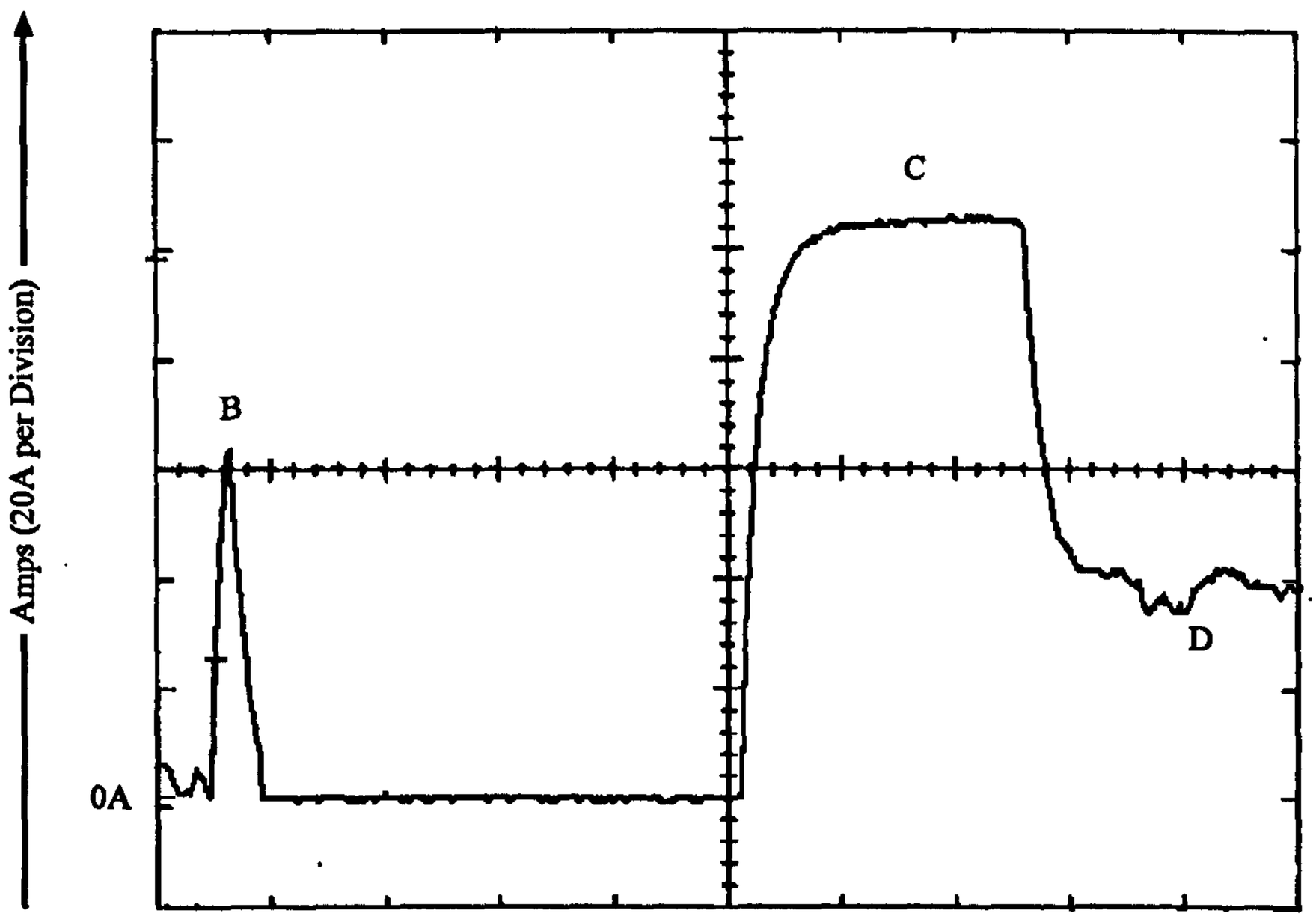


Figure 4.4 Trace Showing VN20 Destruction

From Figure 4.4 it can be observed that the device first manages to contain the rise in current due to the short circuit and so turns itself off (this is indicated by point B in the figure). After the die cools sufficiently, the device turns on for a second time. During

this second turn on sequence control is lost and the current rises to approximately 110A (see location C) at which point the device is destroyed. The falling current towards the end of the trace as indicated by point D, is a result of the die rupturing to an eventual open circuit. It was not possible to determine the exact mechanism that gives rise to the eventual destruction of the device; however, the large fault current and the cyclic thermal stresses induced by the protection strategy are considered to be instrumental.

4.4 Conclusions

Both of the protection strategies currently used in smart power products have been evaluated by experimental testing of a number of commercially available devices. The products that rely on monitoring load current to identify an overload have been found to be reliable and to rapidly isolate a fault which caused the current overload condition. However, for reasons that will be more fully explained in Chapter 6, this fast response time would be problematic in an aircraft power distribution environment since it would be the likely cause of countless nuisance trips. Similarly the fixed trip levels would make the close co-ordination of protection devices difficult to achieve in practice. By contrast, the method of protecting the device using the die temperature measuring strategy does have the advantage of greater insensitivity to nuisance tripping. Unfortunately the devices tested using this protection strategy were demonstrated to be unreliable. Similarly the devices tested had an integral gate drive to facilitate operation as a high side switch. This utility prevents the device from being driven linearly to facilitate fault current limiting.

The manufacturers of smart power switching devices have targeted the automotive industry as the major market for this type of product. Consequently the maximum voltage rating for these devices is limited to 60V.

Finally from a performance standpoint the inclusion of control circuitry and a temperature sensor in the die area has the unwelcome effect of increasing the device on

resistance $R_{DS(on)}$ when compared to that of an identical device having the same die size but without the control circuitry. The reason for this increase relates to the fact that the circuitry takes up space on the die which would otherwise be used to usefully conduct Drain Source current. Since this space can be as much as 20% of the total active die area [35] it means a correspondingly fewer number of cells to share this current, so resulting in a larger $R_{DS(on)}$. Solutions to overcome this problem based on increasing the die size or number of dies will inevitably increase system cost and may impact on the overall SSPC size.

Chapter 5

Power MOSFET Destruction Mechanisms

5.1 Introduction

In order to utilise a power MOSFET as the series pass switching element of an SSPC implementation it is important to understand the principal ways in which power MOSFET's can be destroyed. This chapter examines the physical phenomena that can cause destruction of a MOSFET device and then discusses some general control strategies aimed at avoiding such occurrences.

5.2 Causes of Power MOSFET Destruction

An examination of a manufacturer's specification for a commercially available power MOSFET will reveal a number of parameters relating to maximum operational limits for that device. If the device is driven in excess of these limits device destruction may occur. Despite the fact that many of these limits relate to quantities such as voltages, currents and power dissipation, it is ultimately thermal limitations which are responsible for device destruction. Thermal limits can be breached in the following ways:-

- Exceeding the maximum specified drain to source voltage.
- Exceeding the maximum specified drain source current.
- Exceeding the maximum specified device power dissipation.

5.2.1 Excessive Drain Source Voltage

If the gate of a power MOSFET is subjected to a voltage which is below its threshold voltage V_T (i.e. it is fully turned off) then ideally no current should flow from drain to source. In reality however, a very small current known as 'leakage current' will be detected. If the voltage between the drain and the source is steadily increased, a point will be reached whereby this leakage current will suddenly increase dramatically with a small change in the applied drain source voltage. This point is commonly referred to as the drain to source breakdown voltage or $V_{(BR)DSS}$ and is a specified parameter for all commercially available power MOSFET's.

There are a number different phenomena that can cause this breakdown condition to occur in a MOSFET [41][42]. These phenomena are :

- Avalanche breakdown; this breakdown is the dominant effect in commercially available power MOSFET's, and occurs when the electric field in the vicinity of the body-drain pn junction increases to a critical value.

- Reach-through breakdown; this breakdown is a special case of avalanche breakdown which is caused by the depletion region in the n- type epitaxial layer reaching the heavily doped n+ substrate.

- Punch through breakdown; this breakdown occurs when the depletion region of the reverse biased body to drain junction reaches the heavily doped n+ source diffusion.

- Dielectric breakdown; here the electric field in a dielectric layer such as silicon dioxide or silicon nitride exceeds the dielectric strength of the material. This field causes very large currents to flow through the dielectric and can permanently alter its insulating properties.

Although the different causes of breakdown have been identified, in modern power MOSFET's Dielectric breakdown has been eliminated as potential cause of normal breakdown [42]. Likewise Reach-through breakdown and Punch-through breakdown are rarely observed owing to the fact the power MOSFET is designed to be avalanche breakdown limited.

5.2.2 Avalanche Breakdown

This phenomena, as its name implies, is a sudden avalanche of mobile carriers caused by the increased electric field present within the depletion regions at the body drain pn junction. Electrons or holes that enter the depletion regions acquire sufficient energy from the electric field to knock bound valence electrons out of the silicon lattice atoms in that region. If one electron or hole produces on average less than one additional carrier then the leakage current is not increased. If however, one or more additional carriers are produced and these extra carriers each produce one or more additional carriers then avalanching ensues. The depletion regions around the body-drain pn junction must be wide enough so that the mobile carriers can gain sufficient energy from the local electric field to initiate this process.

The mathematics related to this effect is already known from the analysis of gaseous breakdown phenomena and is described in Equation 5.1 [42] :

$$M = \frac{1}{1-(VR/VB)^N} \qquad \text{- (5.1)}$$

where VB is the junction breakdown voltage, VR is the applied reverse voltage and N is the numerical factor which depends on the type of semiconductor crystal used ($3 \leq N \leq 6$ for silicon). As VR approaches VB, M approaches infinity and the junction breaks down.

When avalanche breakdown occurs, the drain source leakage current will rise dramatically and will only be limited by the resistance of the rest of the circuit. Avalanche breakdown is not destructive in itself and most power MOSFET's have as part of their manufacturer's specification an avalanche current rating. However, since the device has no effective control over the magnitude of current conducted during this breakdown period, should the current ever exceed the avalanche rating then device destruction is likely. Destruction under these circumstances will occur from the following:-

- The source bond wire melting due to the localised joule heating caused by the excessive current density within it (see Section 5.2.4).

- The metalisation layer on the top surface of the die melting (usually in the vicinity of the source bond pad) due again to localised joule heating.

- The semiconductor die breaking down due to heating effects caused by the excessive levels of power dissipation in the die (see Section 5.2.3).

If a power MOSFET is used in the role of a switch or circuit breaker this particular mode of destruction could be encountered if it is to deliver power to an electrical load which is inductive (this is normally true for electrical loads which have wound components such as motors and transformers or where the wire lengths in the circuit are long). An inductor in an electrical circuit stores energy in the form of an electro-magnetic field. The amount of stored energy in an inductor is represented by Equation 5.2:

$$W = \frac{1}{2} L I^2 \qquad \text{- (5.2)}$$

where W is the energy stored in Joules, L is the inductor value in Henries and I is the value of current in Amps flowing through the inductor.

In addition to storing electrical energy an inductor will generate a back electro-motive force (EMF) which opposes any change in current flow. The magnitude of this back EMF, measured in volts, and is given by equation 5.3 :

$$V = L\frac{\partial i}{\partial t} \qquad \text{-(5.3)}$$

where V is the Voltage generated across the inductor, L is the inductor value in Henries, and $\partial i/\partial t$ is the rate of current change in the inductor with respect to time. This stored energy and back EMF has a considerable effect on both switching and circuit breaking devices for the following reason:-

With a conventional circuit breaker on occurrence of a short circuit, the current in the breaker increases to a value at which the breaker is commanded to open the circuit. At this point the current will fall to zero. If an inductor is present in the circuit it will generate a back EMF as a product of the rate at which the current fell to zero and of the circuit inductance. The voltage developed commonly causes an electrical arc to be created across the circuit breaker contacts on opening. This arc will be sustained until either the voltage developed across the arc is greater than the source (EMF) voltage or until all the energy stored in the inductor is dissipated in the arc. Despite the fact electrical arcing causes pitting and burning of the contacts and inevitably leads to a reduction in the useful lifetime of the device, it is however useful in absorbing the trapped energy stored in inductive components. If a solid state device such as a MOSFET is used in place of a traditional electromagnetic device, no arc generation can occur in the semiconductor junction. As such, any back voltage generated by an inductor will also be seen across the MOSFET to which it is connected. Should this voltage ever exceed the avalanche voltage threshold of the device, then avalanche breakdown will occur. Under these circumstances if the energy stored in the inductor exceeds the avalanche rating of the MOSFET then device destruction is likely.

Figure 5.2 shows a photograph of a power MOSFET die (IRF340) which has been damaged by uncontrolled avalanche breakdown. In order to produce this damage the device was placed in a test circuit similar to that in Figure 4.1, with the exception that the resistive load was replaced by a 3mH inductor. A circuit current of 50A was maintained for a short period before rapidly turning off the MOSFET (switching time was recorded at under 10μs). Figure 5.1 shows a photograph of an undamaged IRF340 die. From a comparison of the two dies it can be seen the die metalisation has melted around the source bond.

A control strategy aimed at avoiding such a scenario could be one of the following:

- Use a MOSFET with a breakdown voltage larger than the worst case back EMF.
- Limit the rate of change of current during turn off.
- Apply additional circuitry designed to clamp voltages exceeding a predetermined threshold and to dissipate trapped inductive energy.

The first method suggested, that of using a MOSFET with a breakdown voltage exceeding the anticipated worst case voltage, is attractive in that it is simple and requires no further circuitry to implement. The disadvantage associated with this scheme is that the conduction voltage drop across the device will be greater since $Rds_{(on)}$ of the MOSFET increases with increased breakdown voltage (this topic was previously discussed in Section 3.3.6).

The second method suggested, that of limiting the rate of current change during the turn off, is again a relatively simple solution and offers the additional advantage that electro-magnetic interference (EMI) emanating from the MOSFET and associated circuitry is reduced. The main disadvantage connected with this solution is that it will result in a significantly higher power dissipation within the MOSFET during the turn off transition. This factor has added significance when one considers the scenario of a

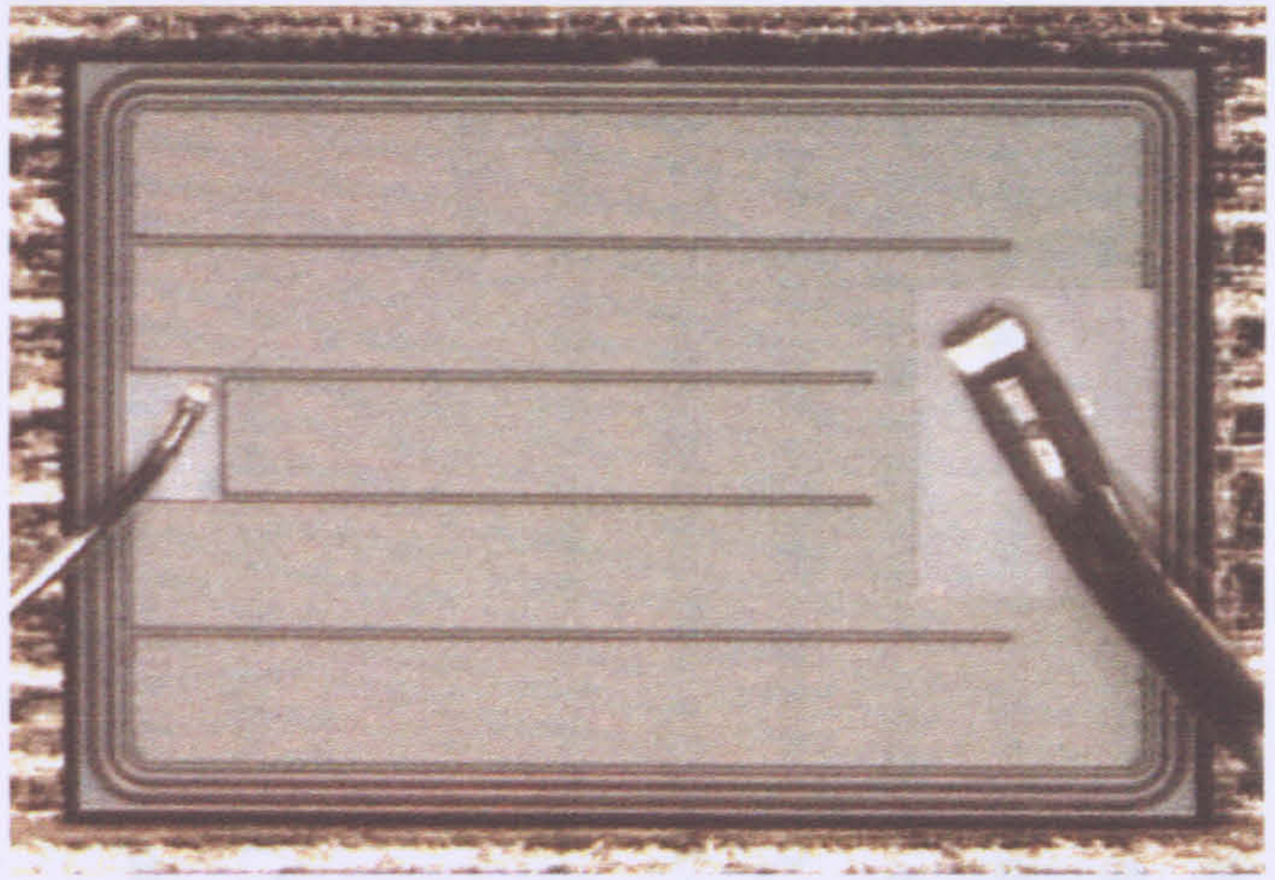


Figure 5.1 Photograph of Normal Die Structure

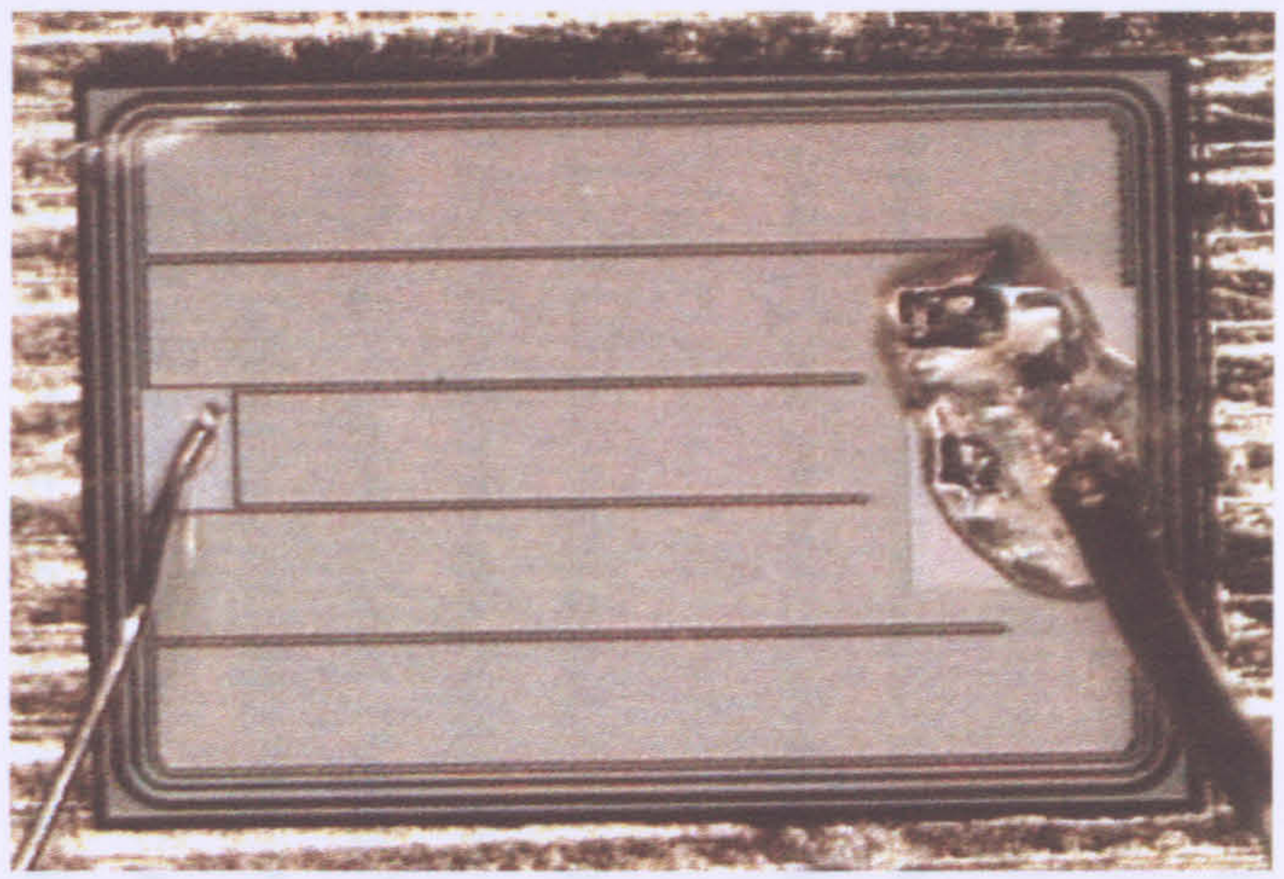


Figure 5.2 Photograph of Die Damaged by Avalanche Breakdown

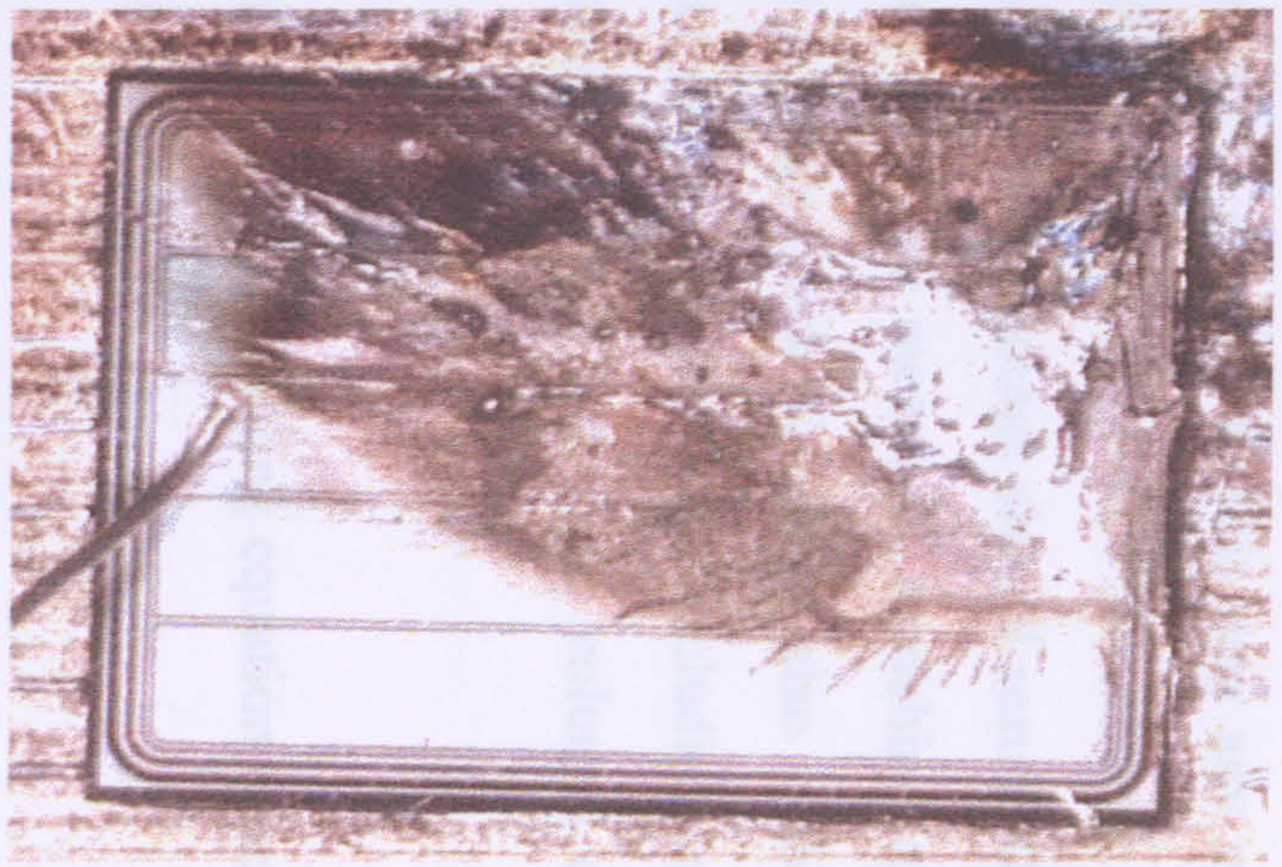


Figure 5.3 Photograph of Die Damaged by Excessive Power Dissipation

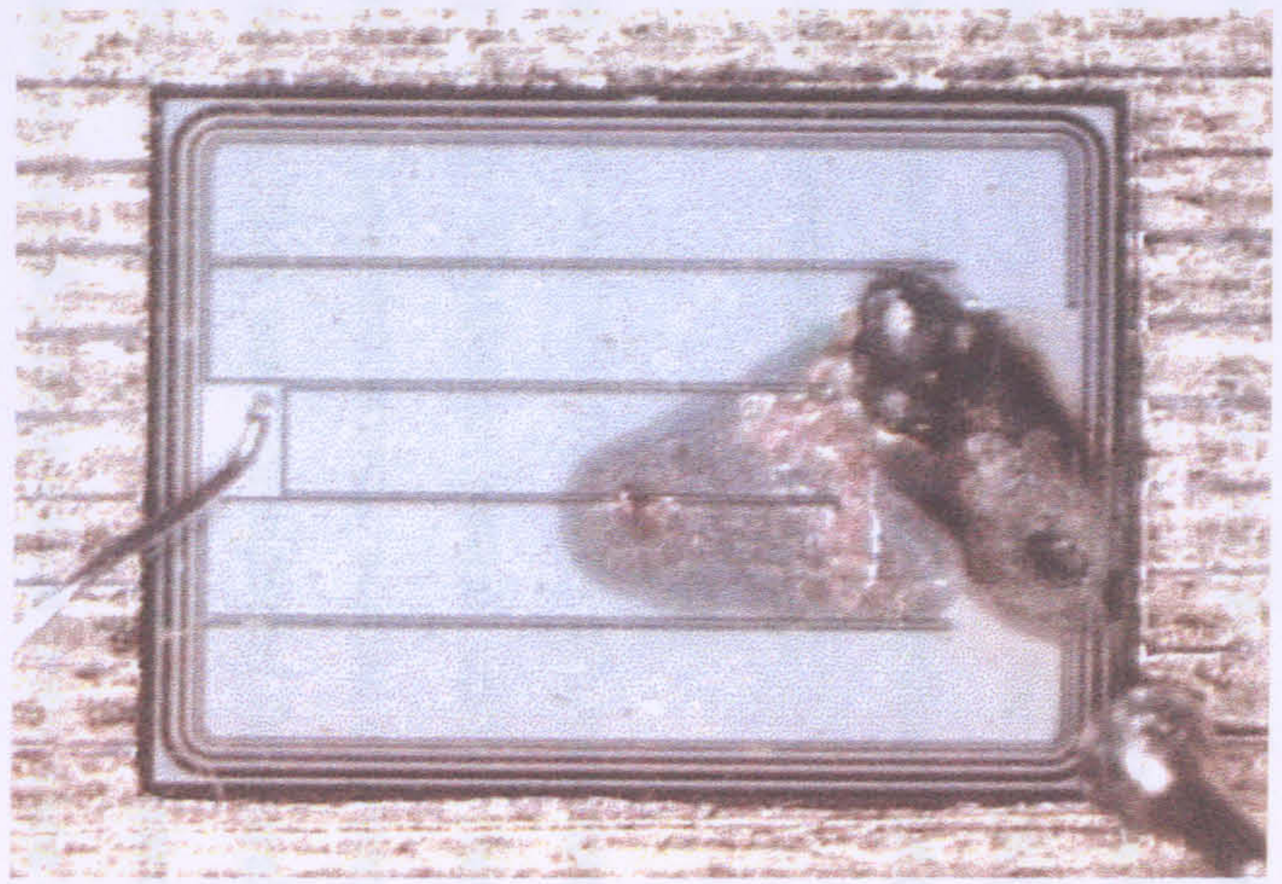


Figure 5.4 Photograph of Die Damaged by Excessive Source Current

MOSFET providing a circuit breaker function. On occurrence of a short circuit the fault current will produce a sizeable heating effect within the semiconductor junction owing to joule heating during the current overload period. If now the junction is subjected to a further period of high power dissipation during the slow turn off the safe operating temperature of the semiconductor may be exceeded. Avoiding such a situation would either mean increasing the size of the semiconductor to accommodate the high power dissipation or beginning the turn off sequence sooner following an overload detection, thus making the circuit breaker more prone to transient nuisance tripping.

The last method suggested, that of providing additional circuitry to clamp excessive voltages, has been suggested by Tian [11] for a Thyristor based circuit breaker. Similarly the use of Metal Oxide Varistors for limiting the arcing across conventional contactors has been described by Paul [43]. This solution was considered favourable by the authors as it is relatively easy to implement and results in little additional hardware. A clamping device such as a Metal Oxide Varistor rapidly reduces its resistance as the voltage across it exceeds a predetermined threshold, and as it does, it diverts much of the current and energy into the suppresser and so to ground. In this way any voltage transient is effectively limited to the threshold voltage and provided the energy of the surge does not exceed the capabilities of the Varistor no damage should result. Despite requiring extra hardware, such a solution does offer the means of switching quickly without the MOSFET having to cope with a large back EMF. It also offers the MOSFET some protection against other sources of excessive voltage including indirect lightening strikes, load shedding and the amplification of harmonic voltages due to resonance.

If the circuit resistance is ignored Tian [11] presents the following equation describing the energy absorbed in a Varistor during an interruption:

$$\varepsilon = \frac{1}{2} LI^2 \left(\frac{V_t}{V_t - E} \right) \qquad \text{- (5.4)}$$

where L is the value of the circuit inductance, I is the fault current, E is the circuit potential and V_t is the Varistor clamping voltage.

The choice of clamping voltage V_t requires a compromise to be made; the greater the clamping voltage then the lower the magnitude of energy to be absorbed and the faster the circuit switching. If the clamping voltage is made to high however the MOSFET will require a larger breakdown voltage and so its $Rds_{(on)}$ will be increased. Tian [11] suggest a V_t /E ratio of between 1.5 and 2.5 as a reasonable compromise. This method of avoiding uncontrolled avalanche is considered to be the most appropriate for the practical SSPC implementation (this item is discussed in Chapter 9) since it does not impact too heavily on the required MOSFET breakdown voltage and is relatively straight forward to implement.

5.2.3 Excessive Power Dissipation

Commercially available power MOSFET's have a specified parameter relating to the maximum permissible continuous power dissipation to which the device may be subject. This limit is however chiefly dictated by the device package and its ability to conduct heat away from the semiconductor die housed within it. As such, the real limit on power dissipation is related to the maximum temperature at which the semiconductor junction can reliably operate. For most commercial devices this is a specified parameter known as Tj_{Max}, the value of which normally lies in the range 150 to 175 degrees C [35][40]. Operating the semiconductor junction at a temperature in excess of this limit can lead to deterioration and destruction of the device.

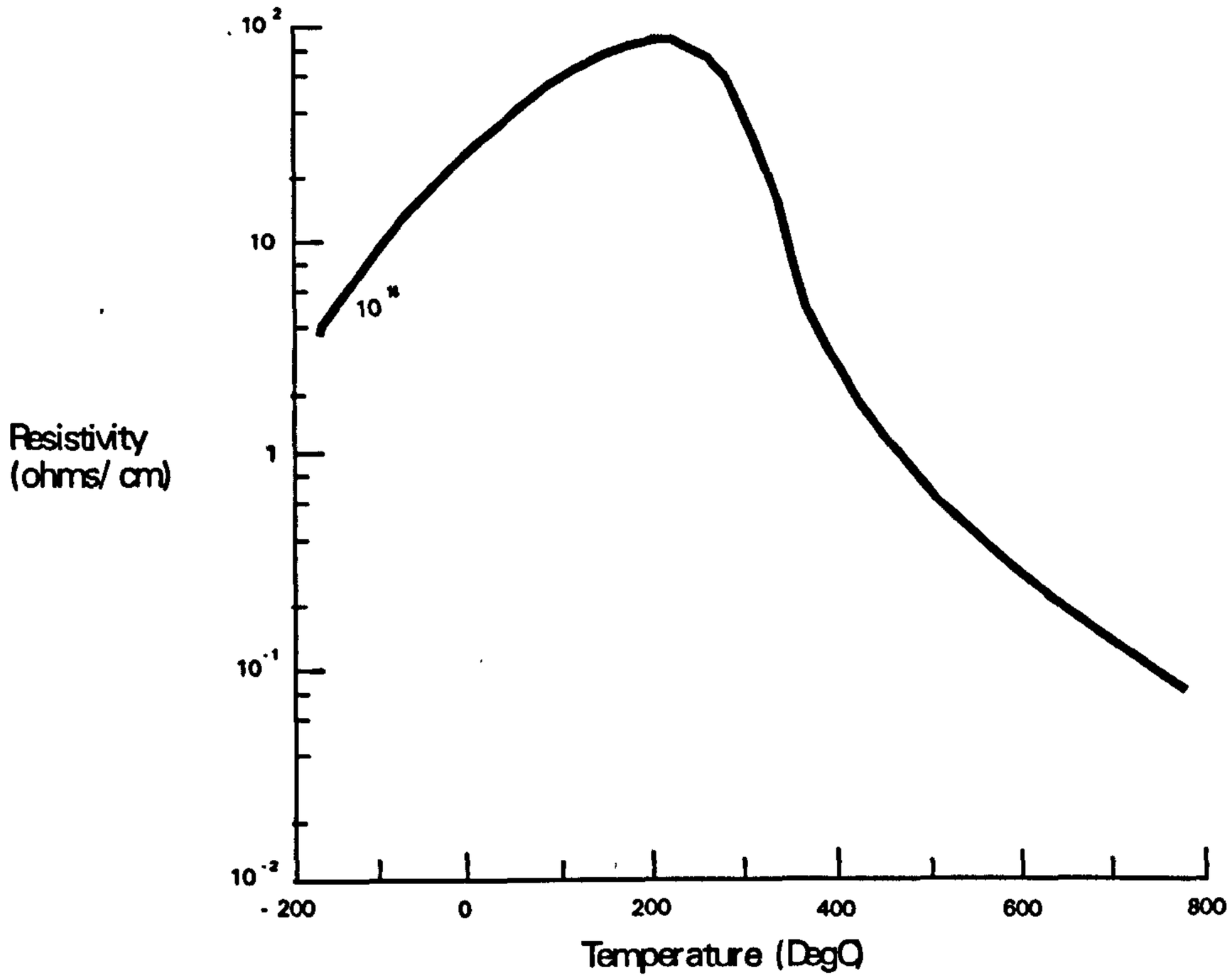


Figure 5.5 Doped Silicon Resistivity as a Function of Temperature

Figure 5.5 shows the variation in the resistivity with temperature for a sample of n-type silicon with a dopant level of 10^{14} cm^3 [45]. At temperatures below 200 Degrees C the temperature coefficient is positive owing to the decrease in carrier mobility as the temperature rises. At higher temperatures (above 200 Degrees C) an 'intrinsic' regime is encountered where due to thermal ionisation both majority and minority carriers are generated and approach their 'intrinsic' (i.e. undoped) carrier concentrations. In this regime resistivity decreases rapidly with increased temperature because of the rapid generation of new carriers which more than offset the decreasing carrier mobility due to the higher temperatures. At temperatures below this intrinsic value negative thermal feedback prevails and any conducting region within the die which had a higher temperature due to a higher current density would exhibit a higher resistance and shed current, thus equalising the current density. If however, the temperature of any conducting area exceeds the 'intrinsic' temperature, the device operation will become unstable due to the negative coefficient of resistivity. This reduction in resistivity will

cause a shift in current into the hot spot, increasing current density and temperature even further. The end result is that the current becomes constricted to a very small area of very high temperature and this temperature is sufficiently high to destroy the device due to melting. High device temperature has also been implicated by Yilmaz [46] as a contributing factor in which the parasitic distributed BJT (formed by the n+ source, p+ channel and n- epitaxial layer) can sometimes turn on. When this happens thermal runaway ensues and quickly leads to the destruction of the device. Figure 5.3 shows a picture of a IRF340 MOSFET die that has been destroyed as a result of a sustained high power dissipation. The device was subjected to a drain source voltage of 200V and then driven in a linear mode of operation in order to supply a constant 10A into a short circuit load. As can be seen from Figure 5.3, severe melting has taken place of both the source bond wire and the die surface metalisation.

When a MOSFET is performing the function of the series pass switching element in a SSPC implementation, this mode of destruction may occur from the excessive resistive heating in the die caused by a prolonged short circuit current overload. Similarly as will be discussed in Section 5.2.4 using the MOSFET to perform fault current limitation will rapidly cause heating of the die. In order to ensure the integrity of the switching device a control strategy is required to measure or predict the junction temperature and turn off the device if it ever exceeds its maximum temperature rating. This topic will be examined in detail in Chapter 8.

5.2.4 Excessive Power Drain Source Current

All power MOSFET's have limits relating to the maximum permissible drain to source current (I_D) for both continuous and pulsed operation. The levels of current stipulated in the manufacturer's limits relate to the maximum current density acceptable in the bond wires and die surface metalisation. Should these limits be exceeded, then the bond wires or die surface metalisation layer will be prone to melting due to localised joule heating. Figure 5.4 shows a picture of a IRF340 MOSFET die that has been subjected to

a drain source voltage of 7V and continuous current of 30 amps. From this photograph melting of the bond wire can clearly be seen. In addition to the melting of the bond wires or die surface metalisation layer, excessive levels of pulsed current may also lead to device destruction through excessive power dissipation in the die. This condition is attributable to the fact that a MOSFET can have a drain current many times greater than that of the maximum continuous current, providing the current pulse is short enough and the average power dissipation within the bond wires or die metalisation is the same as that for the continuous current rating. If however the magnitude of drain current exceeds a device dependent threshold the MOSFET may rapidly be subjected to a very high level of power dissipation and may be destroyed by the same means outlined in Section 5.2.3. The reason for this sudden increase in power dissipation under high levels pulse current is related to the fact a MOSFET has only a finite Transconductance (*gm*).

Transconductance is defined as :

$$gm = \frac{\delta I_D}{\delta V_{GS}} \qquad \text{- (5.5)}$$

where δI_D is the change in drain current and δV_{GS} is the change in gate to source voltage. Note: V_{DS} is constant for this equation.

Since the maximum voltage change between the gate and source is limited to about 15V and the value of *gm* is finite (*gm* is normally in the range of 8 to 16 Siemens for commercially available devices) the drain current will level off or 'saturate' at a certain point even though the device is turned fully on (this of course assumes a sufficiently high voltage between the drain and source so that the current is not limited by the Rds_{on} of the device). Under such circumstances the voltage will increase between the drain and the source with the resultant high levels of power dissipation within the die. When a MOSFET is used as the series pass switching element in a SSPC implementation this mode of destruction could be encountered under two operational scenarios:-

The MOSFET delivering power to an electrical load is suddenly subjected to a short circuit fault down stream of its output. Under such circumstances the current through the MOSFET will be limited only by the output capability of the power source or the combined resistance of the MOSFET Rds_{on} and the network wire.

The second scenario occurs when power is to be delivered to a load which is capacitive (this is normally true for electrical loads which have large filter circuits on their power inputs). A capacitor in an electrical circuit stores energy in the form of an electrostatic field. The amount of stored energy is given by :

$$W = \frac{1}{2} C V^2 \qquad \text{- (5.6)}$$

where W is the energy stored in Joules, C is the capacitance value and V is the voltage across the capacitor.

A current will flow into a capacitor if the voltage across it is increased. The magnitude of this current is given by the equation :

$$I = C \frac{\partial v}{\partial t} \qquad \text{- (5.7)}$$

where I is the current into the capacitor, C is the capacitance value in Farads, and $\partial v/\partial t$ is the rate of voltage change across the capacitor with respect to time.

If a MOSFET is used to power a capacitive load the current demand into the capacitor can be relatively large (e.g. a rate of voltage change of 20V/μs into a 100μF capacitor results in an instantaneous current of 2000A). Such currents can exceed the pulsed current rating of the MOSFET resulting in possible destruction of the device. A control strategy aimed at preventing such destruction caused by excessive drain source current could be one of the following:

- Use a MOSFET or a number of paralleled MOSFET's with a continuous and pulsed current rating larger than that of the anticipated worst case current.

- Limit the rate of change of voltage to the load during turn on.

- Use the MOSFET to limit the current supplied to the load.

The first strategy is likely to have serious impact on both the size and cost of the SSPC. This is due to the fact that in real aircraft implementation the instantaneous turn on current or fault current could be many hundreds of amperes. Likewise, for reasons that will be discussed in Chapter 6 this high current may need to be maintained for a significant period of time to avoid the occurrence of nuisance tripping by the device. To make the MOSFET switch robust enough to cope with worst case high current conditions is likely to render any design uneconomic.

The second suggestion would offer a degree of protection when powering a capacitive load. This solution would not however, provide any protection from the excessive current induced by a short circuit whilst turned fully on.

The final strategy and the one considered the most appropriate is based on using the MOSFET in its linear region to actively limit the current to the load should it exceed a predetermined threshold. Limiting the current to a safe level has the advantage in that it is applicable to both current overload conditions induced by short circuit faults and overloads resulting from powering capacitive loads. This method of control does however have a drawback in that the MOSFET could be subjected to very high levels of power dissipation in the instance where it is actively limiting the current flow (i.e. the MOSFET would have the full supply voltage across it while passing the full load current). In order to protect the MOSFET from this eventuality it is crucial that accurate temperature measurement or prediction to the MOSFET die be applied in order to turn off the device when the die has reached its maximum working temperature. This topic will be discussed in length in Chapter 7.

5.3 Conclusions

This chapter has provided an examination of the mechanisms that cause destruction of a power MOSFET. It has also discussed the operational scenarios to which an SSPC could be subject that could result in one or more of these modes of destruction.

It has been concluded that clamping any voltage transient across the power MOSFET to a safe level by virtue of a Varistor is a suitable method of avoiding uncontrolled avalanche breakdown. Similarly, limiting the fault current to a safe level by driving the power MOSFET into a linear mode of operation is a feasible way of protecting the source bond wire and die surface layer from the melting caused by an excessively high current density within these items. Finally, a strategy has been proposed for protecting the MOSFET against the damage which can occur if the die temperature exceeds its maximum operational limit. The strategy is based on the notion of tracking the die temperature of the device and turning the MOSFET off if its die temperature is excessively high.

Chapter 6

Digital Implementation of Circuit Breaker Characteristics

6.1 Introduction

One problem that needs to be addressed in the design of an SSPC is the complex issue of how to implement the true current-squared-time (I^2t) wire protection trip characteristic which is intrinsic to the older thermal-magnetic circuit breaker. This chapter examines the requirement for true I^2t wire protection and discusses briefly the protection and coordination concepts applied to power distribution systems. As an aid to the understanding, attention is focused on the simple mechanism thermal circuit breakers employ to perform this important function. The chapter then goes on to contrast two differing approaches to solving the problem. One approach being to model the I^2t function as an analogue circuit and the other approach involves modelling the problem using two novel digital algorithms. The merits and disadvantages of each method are explored.

6.2 Protection and Coordination Concepts

When an overload fault occurs within a power distribution system, over-current protection devices are used to isolate only the section of the system affected by the fault, so the remaining system can continue to operate normally. The device has the task of safeguarding the wiring to the affected load downstream of the protection device and equally protecting the power source upstream. Since faults can occur anywhere in the electrical system many protection devices are normally required. These devices are

located such that a single device or, if necessary a combination of devices, operate to isolate a fault.

Good practice dictates that the isolated area must be as small as possible and only the device nearest the fault should operate to perform this task. In addition, the possibility of a protection device not working must be considered. If this happens, the next upstream device or combination of devices must operate to provide a coordinated backup protection. Time discrimination between successive devices provide the necessary means for this coordination of protection.

The protection device should have the attributes of safeguarding the system components from sustained overloads whilst being insensitive to the transient power demands experienced when powering loads such as motors or filament lamps from an initial off state (these devices typically require a starting current 7 or 8 times steady state current as illustrated in Figure 6.1).

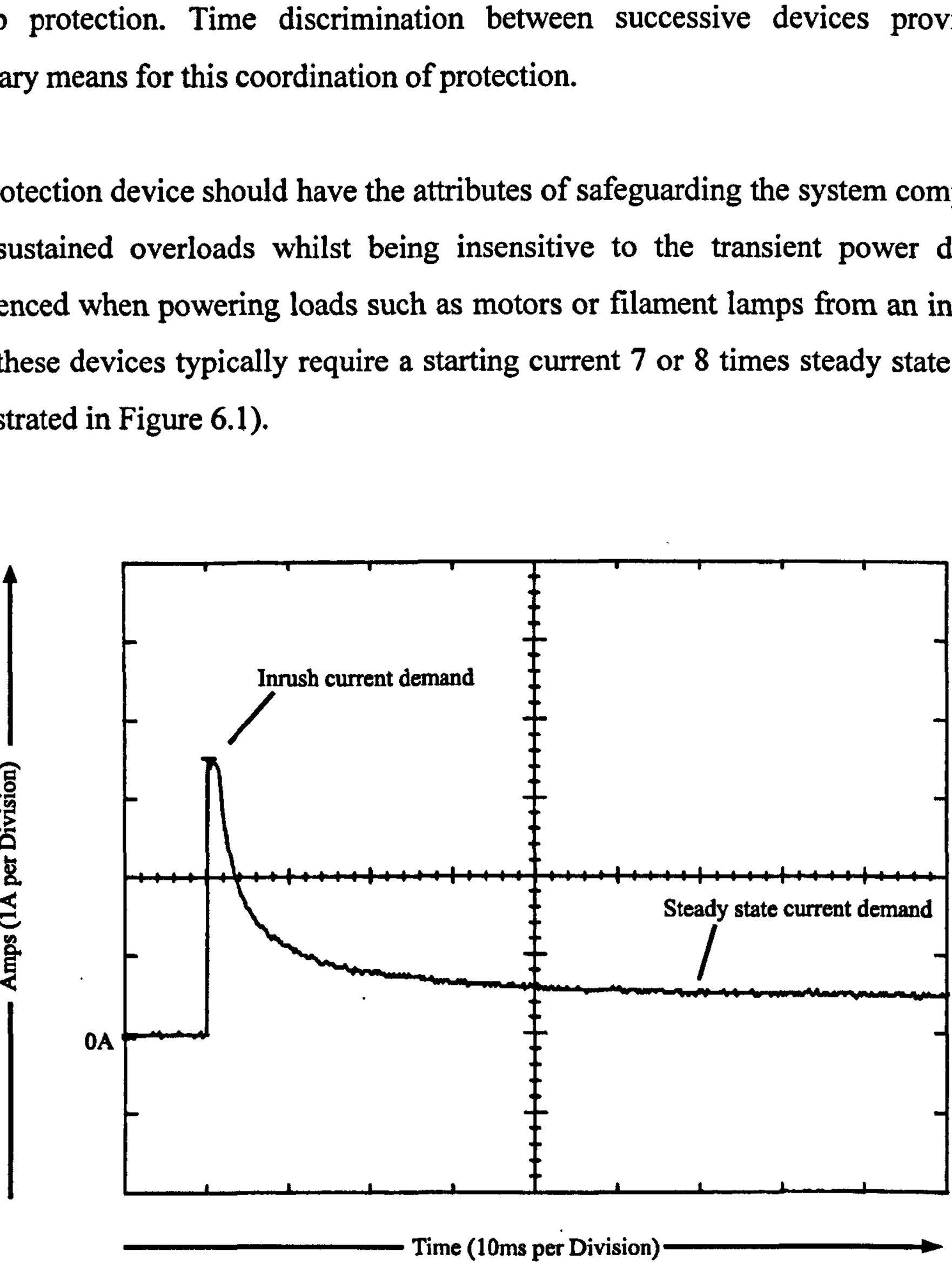


Figure 6.1 Filament Lamp Inrush Current

To achieve this insensitivity the protection device should continue to deliver power under overload conditions for as long as it is safe to do so. The time it can maintain this overload current safely is dictated by the current rating and heating characteristics of the downstream wire the device is protecting.

6.3 Over-current Characteristics

Thermal-magnetic circuit breakers like simple wire fuses have inverse time-current characteristics. This means the larger the overload current the shorter the time to trip. Such devices conform to the constant I^2t which was recognised by Meyer [47] who stated that "I^2t is a quantity which is inherent in any metal". It describes the energy capacity of a metal conductor with respect to the heating generated by an electrical current flowing through it. Hence, I^2 (the square of the current) represents a heating function and t represents the time to reach a critical energy level (trip time). The time lag inherent in the formulae is a function of the conductor material and its cross sectional area. This constant however only represents part of the problem, since it is obvious the device would eventually trip at any non-zero current flow, whereas, the desired characteristic is that the device will never trip if the current is below a certain value. In a thermal circuit breaker or fuse this is achieved by allowing the heating element to lose a certain amount of heat to the surroundings which may be regarded as an infinite heat sink. The loss of heat can be considered to conform to the Newtonian cooling law i.e. :- 'the heat transmission across a surface can be considered proportional to its temperature rise above ambient'.

Thermal circuit breakers consist of a bimetallic strip which bends when heated by the load current flowing through it. Continuous overload currents will cause the bimetal to deflect and eventually to trip the circuit breaker. One can view the simple thermal circuit breaker as an analogue computer since if it is rated correctly to the downstream wire, it models the heating taking place within that wire (since all metals have an I^2t constant) and will trip when the wire temperature exceeds its thermal limit.

Unfortunately this mechanism is not present in an SSPC and consequently must be synthesised using an appropriate technique.

6.4 Electronic Representations of the I^2t Characteristic

At present, current versus time curves are used to describe the typical operation of a protective device [48][49]. For a given circuit breaker these characteristics are usually published as bands on a log/log graph as shown in Figure 6.2.

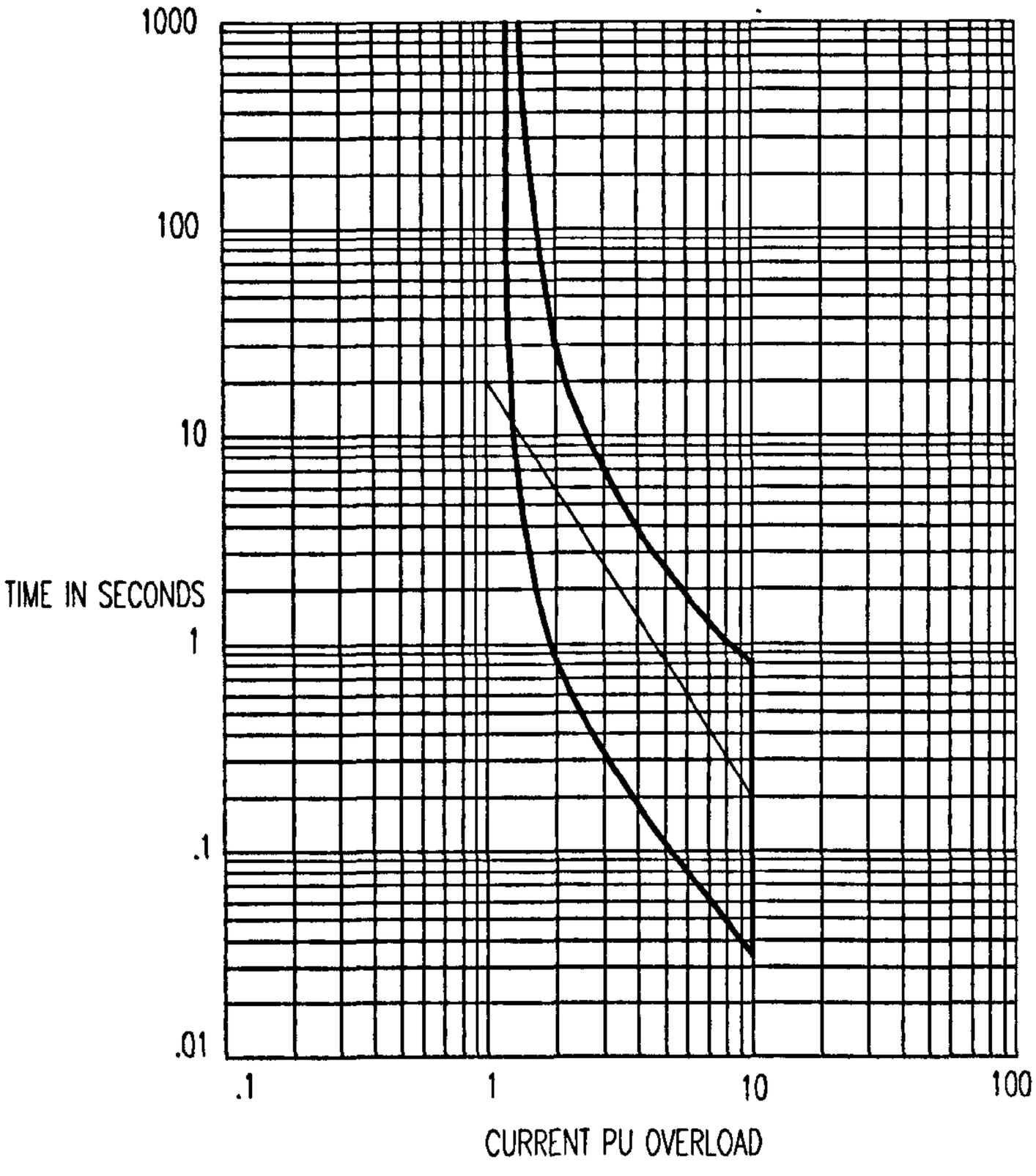


Figure 6.2 MS3320 Time to Trip versus Load Current

The vertical axis represents the time to trip (normally in seconds), and the horizontal axis represents the load current either as an absolute value or a per unit overload 'PU' (i.e. actual current/nominal current). The band represents the bounds of acceptable

behaviour and where a tolerance has been applied (this tolerance is due to inaccuracies caused by mechanical deficiencies and the effects of ageing [50]). The lower edge of the band indicates the minimum time duration at a specified current in which a device may initiate a trip. For all points below this, the device should never trip. The upper edge of the band indicates the maximum time duration at a specified current for the device to initiate a trip. If one were to continue the slope of the curve so that it intersects with the 1 PU current line (see the fine line in Figure 6.2) the time read from the vertical axis at the point of intersection represents the thermal time constant of the protection device.

For an electronic I^2t circuit the problem of defining the device is this:-

This graphical method of specifying a protection device has been used for a great number of years, consequently all circuit breaker manufacturers provide trip curves for their circuit breakers in this format [51]. The electrical equipment manufacturers likewise are used to this method of specification and often detail their requirement for a wire protection device on the basis of what has been empirically found to be acceptable on previous generation equipment. It is highly probable therefore that the only design specification material the designer of the I^2t circuit will ever have is this current versus time trip curve.

The problem arises because in a sense the current versus time curve is only half a specification, in that it details quite precisely the steady state or overload response of the trip device, but contains no explicit information relating to what should happen when the device was subjected to a below trip overload, which has since gone away (i.e. as in the case of the inrush characteristic many loads exhibit when energised). This factor is important, since as previously mentioned the protection device should model the temperature of the downstream wire it is protecting. A previous non-trip current overload will raise the temperature of the wire above nominal for a period of time. Should a second sustained overload occur during this same period, then the protection device should trip in a shorter time than it otherwise would when subjected to just the second overload, since the downstream wire is already at a raised temperature.

More fundamentally the trip times are derived empirically under test conditions where the device is subjected to an over current with no initial load [50]. In practice the device may already be conducting a steady state current when the overload occurs, as such the time to trip for the overload current will again be shorter because the wire temperature is already raised.

A thermal circuit breaker models this to the greater extent, since like the wire it is protecting it is made of a metal strip which when subject to heating by the overload current has a thermal memory similar to that of the downstream wire. An electronic solution built to implement a protection device specified using the time versus current curve could adequately meet the specification but offer poor protection in reality since it need not consider the thermal memory issue as the device specification has no explicit requirement.

An example of such an implementation has been presented by Balasubramanian [52]. Similarly one could adequately meet the requirements of BS142 [53] without any thermal memory. This standard does attempt to address the issue however by specifying a strategy of using two trip curves, namely, a 'cold' and a 'hot' trip response. The cold response is used during the period when the electrical load is first powered and the downstream wire is heating. The hot response is intended to be used for the remaining duration and differs from the cold response in that it models preheating on the downstream wire. Consequently the trip times used for comparable overload current levels are shorter than for the cold trip response. Although this technique goes some way to addressing the thermal memory issue a practical electronic device should however both model the wire heating and cooling in order to provide the necessary degree of protection.

6.5 Simple Model of Wire Heating

As a first step in developing a solution to the I^2t problem it is necessary to create a general form describing the heating which takes place within a wire when it is carrying an electrical current.

Consider a wire of unit length carrying a current *(I)* for a time greater than zero *($t > 0$)*.

Its temperature at time t is:

$$T_a + \Delta T_{(t)} \qquad \text{-(6.1)}$$

where T_a is the ambient (starting) temperature and ΔT is the temperature rise due to the electrical current.

Clearly -

$$\Delta T_{(t)} = CV \int_0^t (P_{in} - P_{out}).dt \qquad \text{-(6.2)}$$

where C is the thermal capacity of the wire material, V is the volume of the unit length of wire, P_{in} is the power into the wire and P_{out} is the power out of the wire.

Pin is due to the resistive heating so

$$P_{in} = I^2 R \qquad \text{-(6.3)}$$

where I is the measure of current conducted within the wire and R is the resistance of the unit length of wire.

P_{out} is the heat loss to the surroundings due to conduction, convection and radiation. A simple model assumes the heat loss is proportional to the temperature rise of the wire above ambient.

If the wire temperature were at ambient at $t=0$ then

$$P_{out} = K\Delta T_{(t)} \qquad \text{-(6.4)}$$

where K is the coefficient of heat loss.

Hence -

$$\Delta T_{(t)} = CV\int_0^t \left(I^2R - K\Delta T_{(t)}\right).dt \qquad \text{-(6.5)}$$

If I and R are constant -

$$\Delta T_{(t)} = aI^2t - b\int_0^t \Delta T_{(t)}.dt \qquad \text{-(6.6)}$$

where $a = CVR$ and $b = CVK$ using the notation above.

The solution to this is -

$$\Delta T_{(t)} = \frac{c}{d}I^2\left(1 - e^{-bt}\right) \qquad \text{-(6.7)}$$

where c and d are constants.

If c and d are known (which in reality would normally not be the case), the time to achieve a given temperature rise for a particular current (I) can be calculated. In practice

however, a wire will be rated for a maximum continuous current which will result in a maximum temperature rise that can be tolerated before damage to the wire, or wire insulation will occur. Obviously it is the absolute temperature that can be tolerated that matters, therefore the maximum ambient operating temperature plus the maximum temperature rise due to the current flow must not exceed this limiting temperature. This situation is represented in the model by -

$$\lim_{t\to\infty}\left\{\Delta T_{(t)}\right\}=\lim_{t\to\infty}\left\{\frac{c}{d}I^2\left(1-e^{-bt}\right)\right\} \qquad \text{-(6.8)}$$

consequently we have -

$$\Delta T_{\max}=\frac{c}{d}\left(I_{rated}\right)^2 \qquad \text{-(6.9)}$$

Where ΔT_{max} = the maximum allowable temperature rise, and I_{rated} is the maximum continuous current for the wire. The time to trip for current overload protection is the time taken to reach ΔT_{max}, therefore, substituting for *T(t)* in Equation 6.7 from Equation 6.9 gives -

$$I_{rated}=I^2\left(1-e^{-bt}\right) \qquad \text{-(6.10)}$$

or

$$t=\frac{1}{b}\ln\left(\frac{1}{1-\left(\frac{I_{rated}}{I}\right)^2}\right) \qquad \text{-(6.11)}$$

Where 1/b represents a time constant.

6.6 Method 1 - Analogue Solution to the Problem

As previously discussed, any electronic implementation of the I^2t characteristic must not only provide the current overload v time to trip characteristic graphically specified, but must also provide the thermal memory which is intrinsic to the thermal circuit breaker. Should this thermal memory requirement be ignored, the protection device could at best be prone to nuisance tripping or at worst offer potentially little protection to the wire.

It is interesting to note that Equation 6.10 has the same form as:

$$V_C = V_i\left(1 - e^{-\frac{t}{rc}}\right) \qquad \text{-(6.12)}$$

which describes the voltage on a capacitor when a resistor-capacitor (rc) network is subjected to a unit step in voltage and where the time constant is given by the product of r and c. This suggests an implementation of an I^2t trip as follows:-

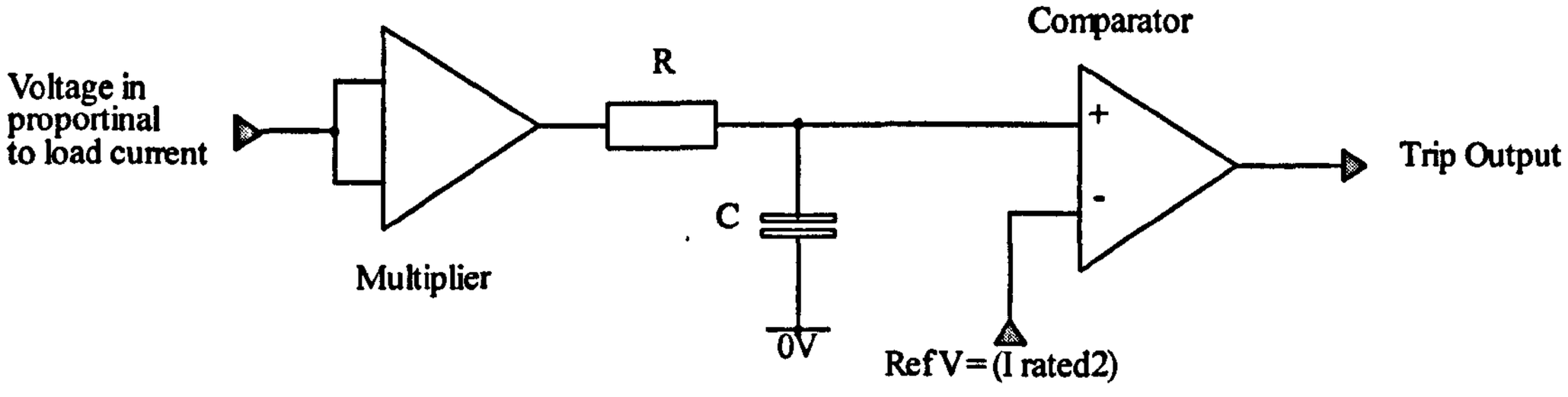


Figure 6.3 Analogue I^2t Implementation

The implementation given in Figure 6.3 uses an analogue multiplier to represent the energy fed into the downstream wire. The resistor capacitor network has a time constant matching the thermal time constant of the wire/thermal circuit breaker (this parameter as previously described is obtained from the time versus over-current trip curve - see Fig 6.2).

The voltage generated across the capacitor represents the actual temperature of the downstream wire, and as such the circuit will issue a trip command if this capacitor voltage exceeds a threshold voltage representing the maximum allowable temperature the wire can reach (i.e. the square of the wire current rating). One important point regarding this circuit is that the capacitor's ability to store charge provides the necessary mechanism to satisfy the thermal memory requirement.

Despite the circuits simplicity, a practical implementation does however suffer from a number of drawbacks which have a direct impact on the circuit accuracy:

A conventional circuit breaker is usually specified to an overload current 1000% above its nominal rating [51] and on certain applications this can extend to 3000% [50]. This means the circuit can be expected to handle an input voltage 10 times greater than the voltage developed for a normal load current. If a voltage 10 times as large is input into the multiplier, then it is obvious since the multiplier is performing a squaring function it will yield a voltage 100 times as large at the output. The positive output voltage swing of most commercially available analogue multipliers (e.g. AD633JN, MPY634KP) are in the order of +11V, consequently the input voltage in relation to normal load current can only be 330mV maximum. The output of an analogue multiplier is prone to offsets of up to 50mV, thus representing a 15% error at 1000% overload and 45% at 3000%. Higher accuracy devices are of course available but the cost is significantly higher and would probably render any solution uneconomic.

The second problem relates to the resistor and capacitor values required to model the thermal time constant of the wire. In most applications this time constant is in the order of 8 to 25 seconds. Generating time constants of this magnitude using resistors and capacitors presents certain problems in that large value capacitors are generally accompanied by either large size or poor tolerance. If the resistor value is instead increased to reduce the required capacitance, the capacitor dielectric leakage current becomes a significant factor and has the effect of distorting the model and making the wire appear cooler than it otherwise would be in reality.

6.7 Method 2 - A Digital Solution to the Problem

With continuing reductions in the cost of microprocessors, microcontrollers and programmable logic devices, a digital approach to characterising trip curves becomes an increasingly attractive option [54][55], both in economic terms and as a way to overcome the accuracy difficulties of an all analogue solution.

The circuit presented in Figure 6.3 may be decomposed into a number of discrete operations, namely:

i, A squaring operation

ii, An integration

iii, A comparison and decision to trip.

All these functions are amenable to digitisation.

The first stage in the digitisation process is to capture the input voltage in a binary form. This operation is normally performed using an analogue to digital converter. The digital value can then be multiplied by itself to yield a value representing the load current squared. This numerical value will then serve as the input into the following algorithm which provides the required first order lag :-

At time *(t)* the temperature of the wire may be expressed as follows:-

$$T_{(t)} = P_{(t)} - \left(P_{(t)} - T_{(t-1)}\right)K \qquad \text{-(6.13)}$$

where T is a voltage representing the wire temperature, P is a voltage representing the sampled value of load current squared, and

$$K = e^{-\frac{sp}{\tau}}$$

where *sp* is the sample period of the iterative cycle and τ is the time constant of the trip curve.

The final operation in the procedure is to compare the value $T_{(t)}$ representing the wire temperature with a threshold voltage value representing the square of the downstream wire rating. If the wire temperature ever exceeds this threshold then the software will issue a trip command.

6.7.1 Test Results for Method 2

The above algorithm was initially implemented on a test system utilising an inexpensive 8 bit microcontroller to perform the digital processing (a later implementation will be discussed in Chapter 9). In addition to performing the I^2t algorithm the microcontroller was also used to command a power switching element comprising of two VN20 solid state switches. These switches could open circuit the current flow from a 26V battery supply to a 6Ω rheostat. A measure of the current was derived from a small (0.005Ω) inline current sensing resistor. The voltage developed across this resistor was amplified and then input into an analogue to digital (AtoD) converter.

A block diagram of this test system is given in Figure 6.4 and a photograph may be seen in Appendix 6.

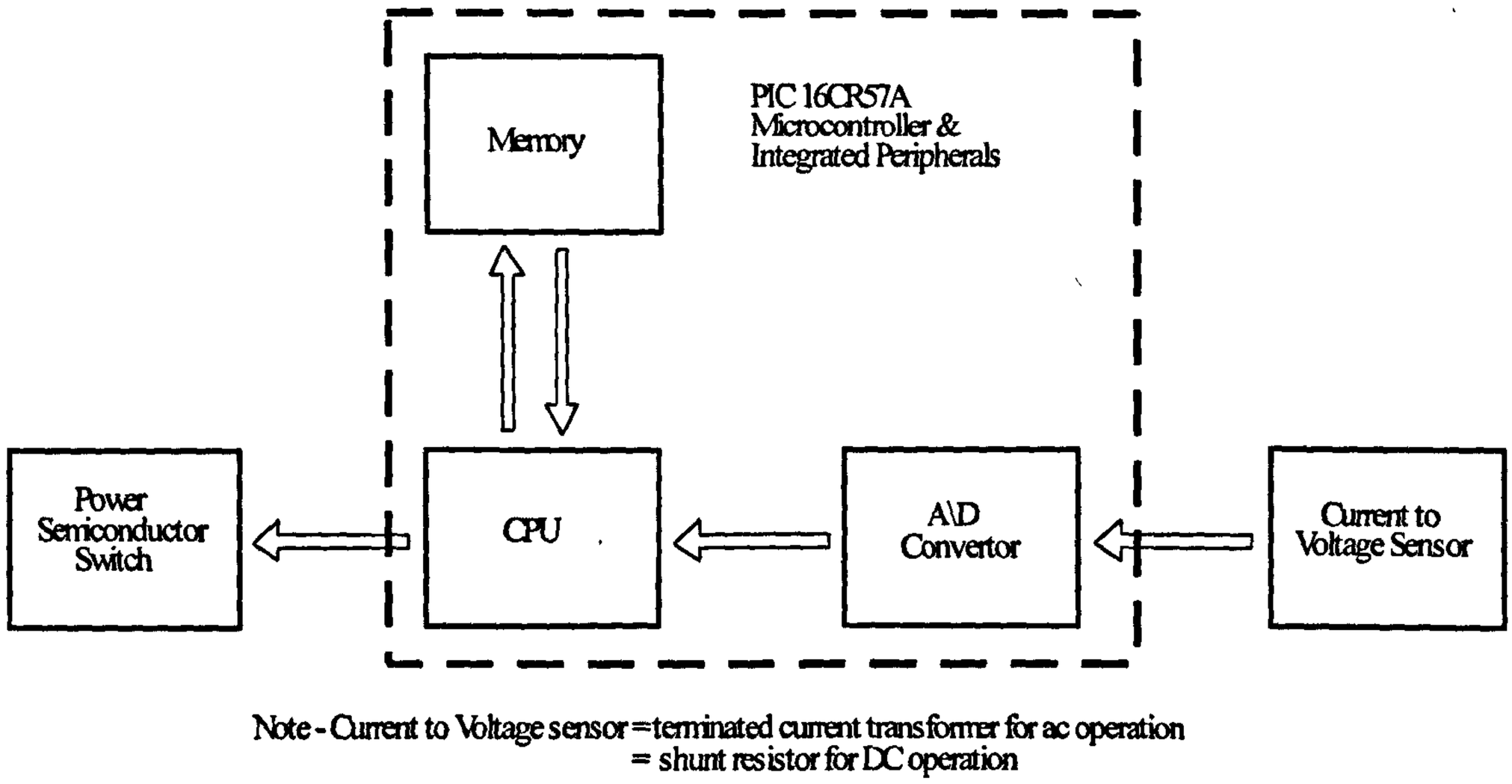


Figure 6.4 - Schematic of Microcontroller Test System

The program constants were configured for a real specification trip curve i.e. a 10A type conforming to the MS3320 standard reproduced in Figure 6.2 (the time constant was measured to be 19.8 seconds). The test apparatus was initially bypassed and the rheostat systematically adjusted to achieve a desired load current. During this operation a Hall effect current probe was used to provide a measure the current flow. The test system was then introduced back into the circuit and the microcontroller commanded to turn on the switching elements. The time taken from this event to the switch being turned off as a result of an overload trip was recorded using a digital timer counter. For trip times in excess of 10 seconds however, the measurement was performed manually with the aid of a stopwatch.

Figure 6.5 presents the results of this test plotted against a theoretical trip response for the 10A MS3320.

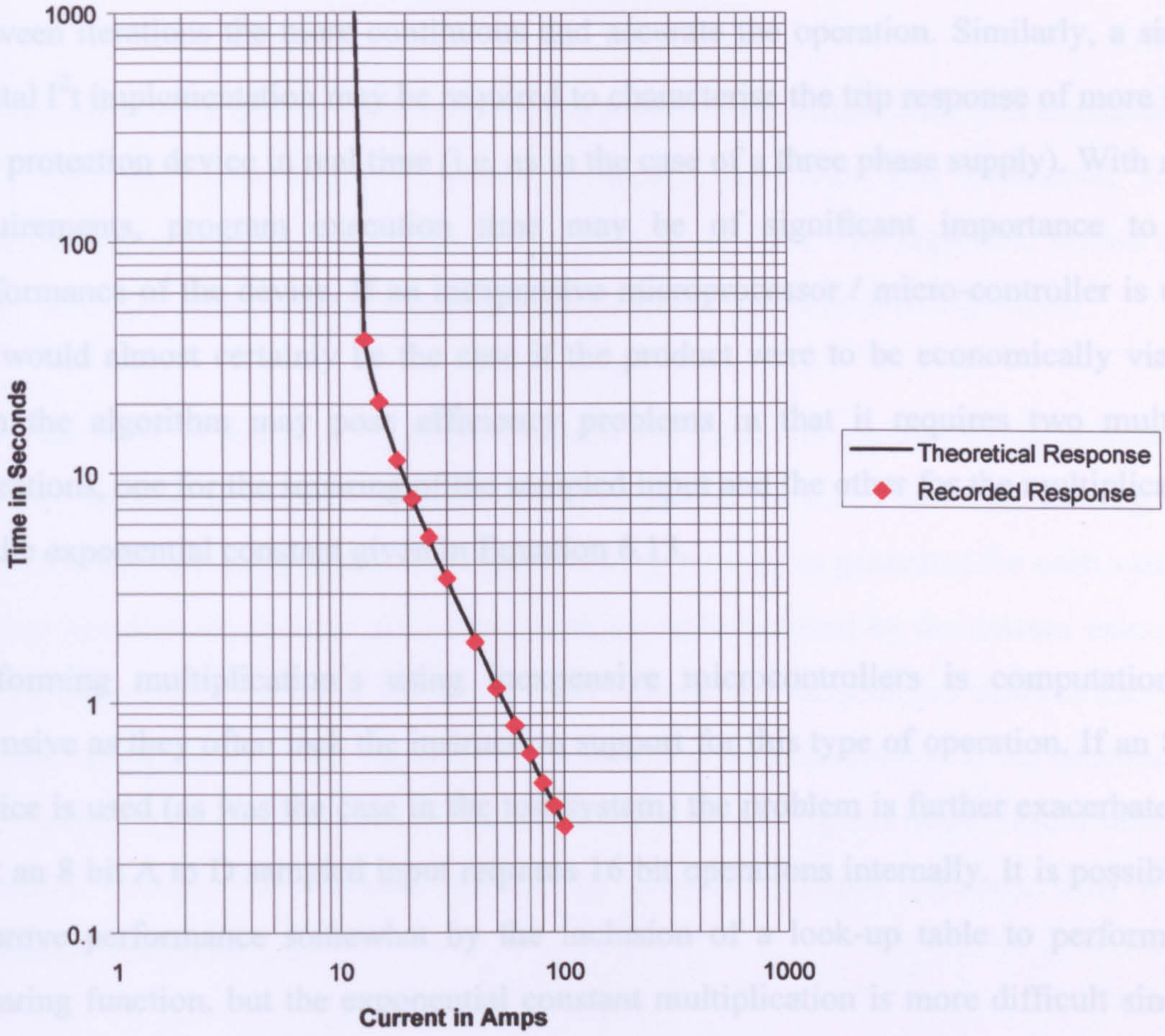


Figure 6.5 -Time Constant Method Results

From a comparison of the trip curve presented in Figure 6.5 and the MS3320 trip curve of Figure 6.2 it is apparent that digital implementation produces a current input versus time to trip function which is well inside the tolerance band of the MS3320 specification.

6.7.2 Performance and Economic Considerations of Method 2

Although the algorithm developed to provide I^2t wire protection has been demonstrated by experimentation, to produce the required trip response there are however a number of implementation issues which should be considered. Since the algorithm is iteratively

performing the function of Equation 6.1, it is obvious the shorter the time duration between iterations the more continuous and accurate the operation. Similarly, a single digital I^2t implementation may be required to characterise the trip response of more than one protection device in real time (i.e. as in the case of a three phase supply). With such requirements, program execution time may be of significant importance to the performance of the device. If an inexpensive microprocessor / micro-controller is used (as would almost certainly be the case if the product were to be economically viable) then the algorithm may pose efficiency problems in that it requires two multiply operations, one for the squaring of the sampled input and the other for the multiplication by the exponential constant given in Equation 6.13.

Performing multiplication's using inexpensive microcontrollers is computationally intensive as they often lack the instruction support for this type of operation. If an 8 bit device is used (as was the case in the test system) the problem is further exacerbated in that an 8 bit A to D sampled input requires 16 bit operations internally. It is possible to improve performance somewhat by the inclusion of a look-up table to perform the squaring function, but the exponential constant multiplication is more difficult since it will always be a number less than 1 and as such will require either floating point or fixed point arithmetic to carry out the calculation. Owing to the lack of dynamic range associated with this multiplication it is not possible to implement a practical look up table to perform the calculation. To this end the best execution time achieved on the test system for a single A to D sample iteration was 520μs.

Another, more minor point of consideration associated with this method is that the extraction of a time constant from a given trip curve is sometimes awkward and time consuming to achieve in practice. The problem is primarily attributable to the large tolerance band displayed on existing trip curves which often make it difficult to determine the correct gradient and ultimately the true time constant value. As such, several iterations are often required before the desired trip response is achieved in practice.

6.8 Method 3 - Another Digital Solution to the Problem

Owing to the performance difficulties of the previous algorithm when it is implemented on simple low cost microcontrollers, a second algorithm was developed which demonstrates a considerably reduced execution cycle time. The algorithm differs from Methods 1 & 2 in the way it characterises the current versus time to trip curve.

Since the curve is simply a function of current and time, it is possible to characterise the curve by reading trip times for each value of current in the x axis and then dividing each time to trip by the sampling period. In this way a constant is generated for each value of current and this can then be stored as a look-up table indexed by the current value. All the trip algorithm need do is sample the load current, use the sampled value to index the corresponding constant and then add this constant to an accumulator. If the accumulator ever exceeds a threshold (given by the time to trip for the highest rated current value i.e. normally 1000% PU overload divided by program sample interval), then a trip command will be issued.

Although this method will generate a trip response in accordance with the specified current versus time to trip curve, the value in the accumulator represents a heating component only and as previously noted a cooling component is also required for correct operation of the protection device. Despite the fact the current versus time to trip curve contains no explicit information relating to this cooling component, it is however possible to make some important assumptions:

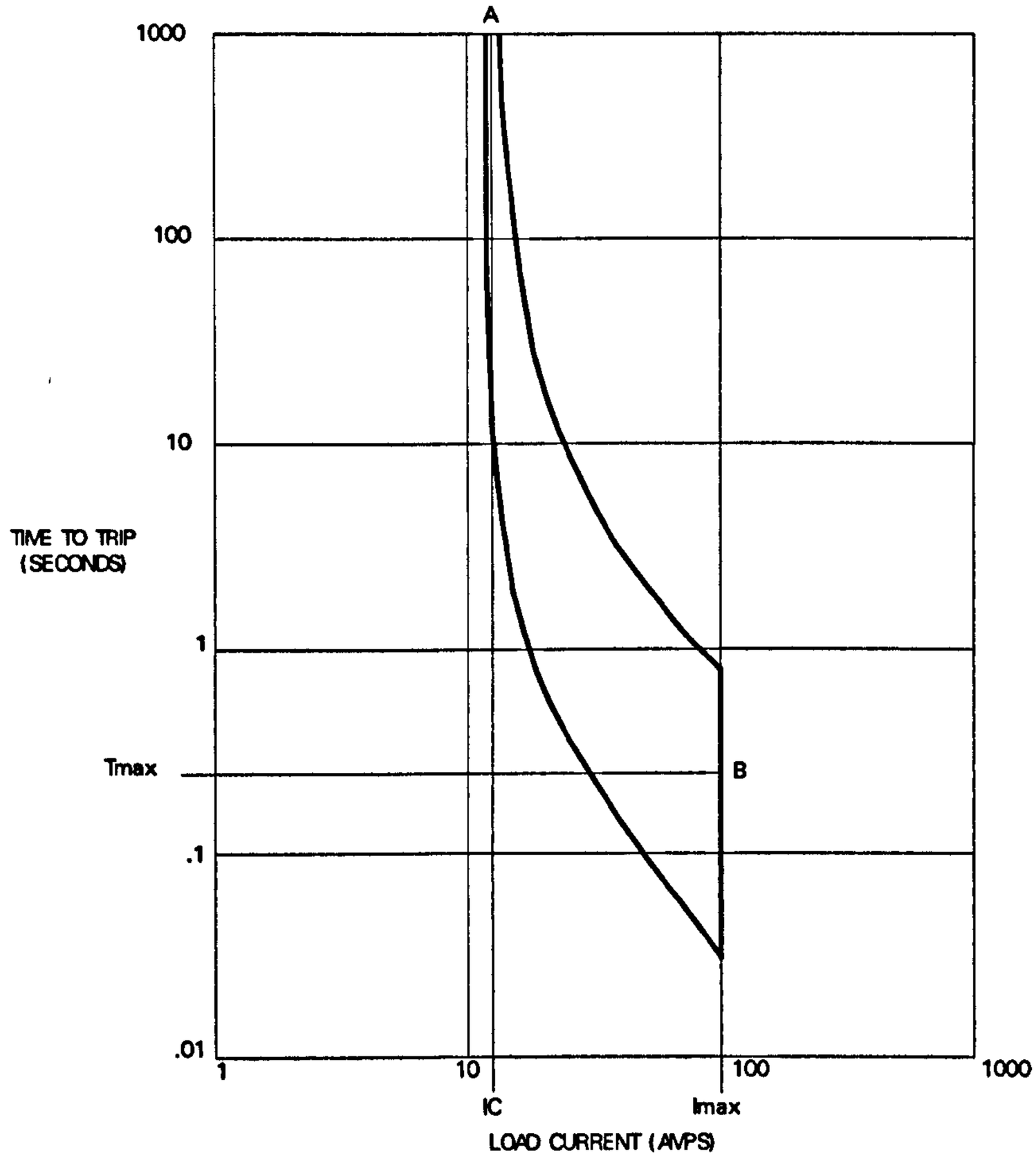


Figure 6.6 - Method 2 Parameter Extraction

At point A in Figure 6.6 on the current versus time to trip curve, the protection device is in a state of equilibrium, that is, at the current value corresponding to point A, the energy into the device is equal to that of energy lost through conduction, convection and radiation.

Using this assumption it is possible to derive a cooling term (Ic^2) as a value of the square of the load current. Since heating is again a function of the square of the load current at the very high values of current over which the protection device is designed to operate (see Figure 6.6 point B) it can be assumed the effects of cooling are negligible.

Using these two assumptions it is possible to solve the problem on a computational engine which performs a numerical integration at a regular sampling time interval using the formulae -

$$\Delta T = \sum_{0}^{t}\left(P_{in} - P_{out}\right) \qquad \text{- (6.14)}$$

where ΔT is the temperature change of the downstream wire, t is the sampling period, P_{in} is the wire heating component, and P_{out} is the wire cooling component.

As the number of samples increases and consequently t→∞, we have

$$\lim_{t\to\infty}\left(\sum_{0}^{t}\left(P_{in} - P_{out}\right)\right) = \int_{0}^{t}\left(P_{in} - P_{out}\right)dt \qquad \text{- (6.15)}$$

by the MacLaurin-Cauchy Theorem. If the constant CV of Equation 6.2 is equated to unity, the right hand side of Equation 6.14 becomes Equation 6.2. Thus these two Equations i.e. 6.2 & 6.14 are equivalent for infinitely small sampling time.

Equation 6.15 can be translated into the following algorithm :-

$$Acc_n = Acc_{n-1} + Heating - Cooling \qquad \text{-(6.16)}$$

where Acc_n is a value representing the new temperature of the wire and Acc_{n-1} is a value representing the old temperature.

The routine will issue a trip command if ever the value of Acc_n exceeds a constant threshold (Acc_{max}). This constant is a product of the square of the maximum load current over which the protection device is to operate $(Imax)^2$, the time to trip for that value of current *(Tmax)* and the sample interval and is thus given by:-

$$Acc_{\max} = I\max^2 * \frac{T\max}{Sample\ Period} \qquad \text{-(6.17)}$$

and

wire heating is simply:

$$Load\ Current_n^{\ 2} \qquad \text{-(6.18)}$$

where n is the sample value.

In addition,

$$Wire\ cooling = Ic^2 * \frac{Acc_{n-1}}{Acc_{\max}} \qquad \text{-(6.19)}$$

6.8.1 Test Results for Method 3

The above algorithm was again implemented on the test system as described in Section 6.7.1 and similarly the program constants configured for the same 10A MS3320 trip curve. The mechanics of the implementation made use of two look-up tables and an accumulator. The first look-up table calculates the heating contribution by converting the value of current I into I^2. The second calculates the cooling contribution by taking the previous temperature representation and converting it in accordance with Equation 6.19. These look-up values are then added and subtracted from the accumulator value respectively. Each time a new pair of heating and cooling values has been included, the summation value is compared to the reference value Acc_{max} and the trip activated if the summation value exceeds the reference value.

The execution time achieved with this algorithm for a single A to D sample iteration was 35μs (including the 10μs A to D conversion time) showing a dramatic improvement over the previous algorithm. The resultant current versus trip time function generated by this heating/ cooling I^2t implementation model is shown in Figure 6.7.

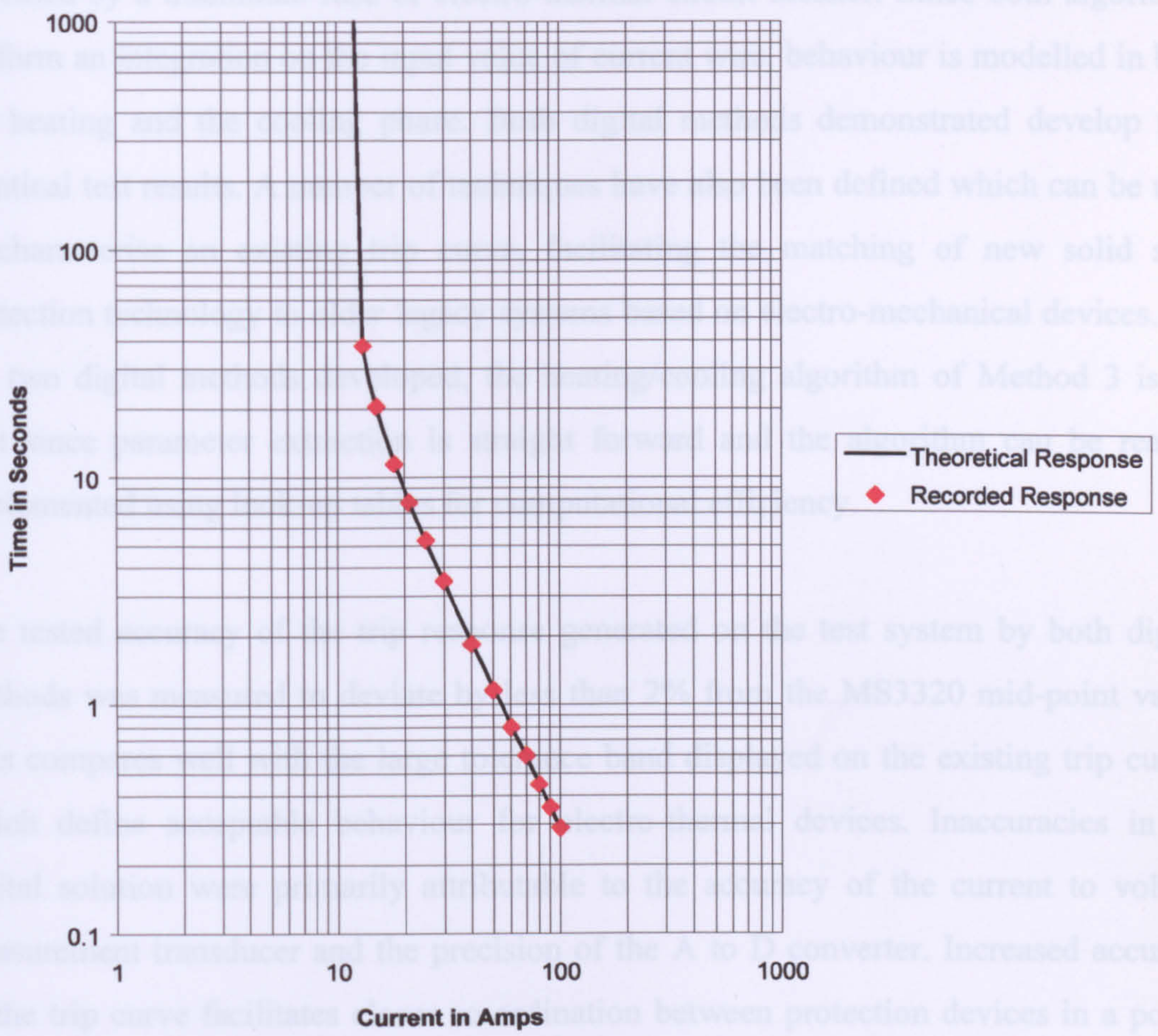


Figure 6.7 - Heating Cooling Method Results

From a comparison of Figure 6.2 with Figure 6.7 it is seen that this digital implementation generates an output response mirroring that of the MS3320 current versus time to trip curve. It is also interesting to note that when the test results from this digital algorithm are compared with the test results of the thermal time constant algorithm (see Figure 6.5) they produce almost identical results, showing that the results are a good practical indication of the theory.

6.9 Conclusions

It has been demonstrated that by using inexpensive digital technology it is possible to provide a solid state power controller with a true I^2t trip function mirroring that provided by a traditional fuse or electro-thermal circuit breaker. Since both algorithms perform an integration on the input value of current wire, behaviour is modelled in both the heating and the cooling phase. Both digital methods demonstrated develop near identical test results. A number of techniques have also been defined which can be used to characterise an existing trip curve, facilitating the matching of new solid state protection technology to older legacy systems based on electro-mechanical devices. Of the two digital methods developed, the heating/cooling algorithm of Method 3 is the best since parameter extraction is straight forward and the algorithm can be readily implemented using look-up tables for computational efficiency.

The tested accuracy of the trip response generated on the test system by both digital methods was measured to deviate by less than 2% from the MS3320 mid-point value. This compares well with the large tolerance band displayed on the existing trip curves which define acceptable behaviour for electro-thermal devices. Inaccuracies in the digital solution were primarily attributable to the accuracy of the current to voltage measurement transducer and the precision of the A to D converter. Increased accuracy of the trip curve facilitates closer co-ordination between protection devices in a power distribution system. This increases the likelihood that only the device nearest the fault will interrupt the supply of power. Likewise, depending on the inrush requirements of the load, it may also allow the current rating of certain power feeders in the system to be reduced, saving both space and cost. The digitally generated trip curve was demonstrated not to be compromised by device temperature variations or the difficulties of accurately generating large time constants using passive components. The digital implementation may also claim an advantage in relation to size and flexibility, since only variables need change to characterise different I^2t curves. The digital methods may also produce a trip response conforming to I^nt where *'n'* can be any index. This feature will facilitate device co-ordination under difficult circumstances e.g. an electrical load

with an unusually large inrush requirement. Finally, although the techniques developed have specifically targeted solid state controllers, existing electro-mechanical contactors (i.e. a power interruption relay) can equally make use of this technology to accurately control their trip point.

Chapter 7

Heat Distribution in a Power MOSFET

7.1 Introduction

In Chapter 5 it was identified that under operational conditions excessive MOSFET die temperature is a potential cause of device destruction. In a current limiting SSPC, power dissipated within the die under short circuit conditions may reach very high levels (>500W) which results in rapid heating of the die and surrounding area. To ensure the integrity of the semiconductor it is necessary to know or to predict its temperature at any point in time and take measures to ensure this temperature never exceeds the upper temperature limit for that device. The details of how this may be achieved, and the associated issues are examined in Chapter 8. However, in order to both calibrate and to validate the accuracy of this temperature monitoring scheme, it was considered necessary to gather data relating to MOSFET die temperature rise under varying levels of power dissipation. Two approaches were taken, the first approach focused on performing a number of experimental temperature measurements on a candidate test device. The second approach was the construction of a detailed thermal model using a custom computer simulator.

7.2 Heat Transfer

Transfer of heat energy may take place by one or more of three known phenomena: Conduction, Convection and Radiation. In the following discussion we briefly examine each of the three heat transfer modes.

7.2.1 Heat Transfer by Conduction

Conduction is a means whereby there is an energy transfer from a region of high temperature to a region of low temperature within a body. This form of heat transfer can be transitional, rotational or vibrational. Fourier [56] has shown that the quantity of heat transferred per unit time by conduction is given by:-

$$q = -kA\frac{\partial T}{\partial x} \qquad \text{- (7.1)}$$

where q is the heat-transfer rate, A is the cross-sectional area, $\partial T/\partial x$ is the temperature gradient in the direction of heat flow and k is the thermal conductivity of the material (k has the units of Watts per Meter per Degrees C). The minus sign is inserted to satisfy the principle that heat must flow downhill on the temperature scale (i.e. heat flows from a hot body to a cooler body). If the system is in steady state i.e., if the temperature does not change with time then the solution to the problem simply involves integrating Equation 7.1 and substituting the appropriate values to solve the desired quantity. If however the temperature of the solid is changing with time the situation is more complex and the equation becomes:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right) + \dot{q} = \rho Cp\frac{\partial T}{\partial t} \qquad \text{- (7.2)}$$

where $\dot{q}$ is the energy generated per unit volume in joules, Cp is the specific heat of the material in joules per kilogram per degrees C and ρ is the density of the material in Kilograms per Meters^3.

Equation 7.2 above is a one dimensional heat conduction equation i.e. heat is conducted in one direction only within the solid.

If heat is conducted in all three co-ordinate directions the equation now becomes:

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+\dot{q}=pc\frac{\partial T}{\partial t} \qquad \text{- (7.3)}$$

and if the thermal conductivity is constant Equation 7.3 is written as:

$$\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}+\frac{\dot{q}}{k}=\frac{1}{\alpha}\frac{\partial T}{\partial t} \qquad \text{- (7.4)}$$

where the quantity $\alpha = k/pc$ is called the thermal diffusivity of the material. The larger the value of α the more rapidly heat energy will transfer through the material.

7.2.2 Heat Transfer by Convection

Convection refers to the conveyance of heat energy from, or to, a body by the movement of a fluid or gas. The heat transfer depends on the velocity of the flow thereby making it a different modelling process to conduction. The convection heat transfer process is expressed by Newtons cooling law :

$$q = hA(Tw - T\infty) \qquad \text{- (7.5)}$$

where Tw is the body temperature, $T\infty$ is the fluid temperature and A is the surface area of the interface. The quantity h is called the convection heat transfer coefficient and it can be analytically modelled in some particular cases or experimentally measured.

7.2.3 Heat Transfer by Radiation

In this mode heat is transferred by electromagnetic radiation and therefore does not require another medium as a means of transferring heat. It has been found that for an ideal black body (a body that at all temperatures absorbs all radiation incident upon it) the total power of radiant flux is given by the equation:

$$q = \sigma A(T_1^4 - T_2^4) \qquad \text{- (7.6)}$$

where σ is the Stefan-Boltzman constant and has a value of 5.669×10^{-8} W/m^2·K^4
A is the surface area of the radiating body, T_1 is the temperature of the radiating body and T_2 is the temperature of the element receiving the radiant heat energy.

Two other factors can be introduced for taking into account that not all the radiated heat will fall on the recipient body and that not all bodies are perfect black bodies. These factors are called the geometric view factor *(Gw)* and the emissivity *(ε)*. The emmsivity is defined as the ratio of the emissive power of an object to the emissive power of a similar object which is a perfect black body. Equation 7.6 can be modified to include these two terms:

$$q = \sigma\varepsilon GwA(T_1^4 - T_2^4) \qquad \text{- (7.7)}$$

Heat transfer by radiation may be very complex and as such the above equation may not accurately model the process.

7.3 Power MOSFET Thermal Model

Most commercially available power MOSFET's have a die mounting arrangement similar to that seen in Figure 7.1.

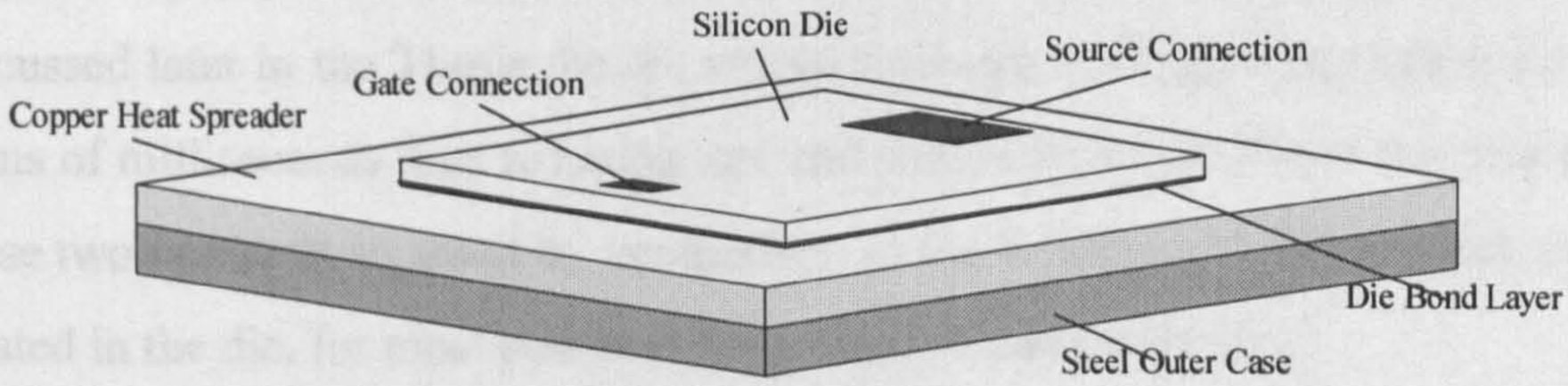


Figure 7.1 Die Mounting Arrangement (TO 3 Package)

In its most elementary form it consists of three components: a silicon die, a thin layer of die attach material and a base, which, depending on the package type may be made up of one or more layers of material.

Heat in a MOSFET die is dissipated in any resistive path through which current flows. The dominant region of heat dissipation is in the die epitaxial layer, which is an area located directly under the top surface metalisation. The epitaxial layer is the active part of the device (the junction) and depending on the voltage rating occupies a depth of between 8μm and 100μm in most commercial devices [57] (the depth of the epitaxial layer increases with increased device voltage rating).

The material surrounding the top and side surfaces of the die are normally of poor thermal conductivity (air, ceramic or plastic resin). As such, the heat generated in the epitaxial layer will be transferred by conduction downwards through the remaining silicon layer (silicon substrate) through the die attach material and into the heat spreading base. From here the heat can be radiated or conveyed away or transferred by conduction into a suitable heatsinking arrangement. It can be shown by using Equations

7.5 and 7.6 that direct heat lost from the die due to convection and radiation is approximately 2.05×10^{-2} W and 1.325×10^{-3} W respectively. This assumes the die is at a maximum temperature of 175 Degrees C above the temperature of the surrounding element and has a top surface area of 2.492×10^{-6} m^2 (i.e. size 4). The heat transfer would be far lower than these figures in reality however, since the die is not a perfect black body radiator (it will be shown later that the die has an emmisivity of 0.45) and as will be discussed later in the Thesis the die would attain such a high temperature for only a few tens of milliseconds thus reducing any convection heat loss. Since the heat transfer by these two modes is so small by comparison to the hundreds of Watts which could be dissipated in the die, for most practical purposes they can be ignored.

7.4 Determination of Temperature Rise by Experimental Means

In order to validate the accuracy of any temperature prediction method or accompanying modelling activity it was considered necessary to perform some experimental temperature measurements on a candidate test device. From the description of the die mounting arrangement given in the preceding section it can be seen that for the heat to reach the outside of the device package it must have first passed through a number of physical layers. For reasons that will be explained in Chapter 8, it is not possible to determine the die temperature at any point in time simply by measuring this outside package temperature on account of the interaction the layers of material have on the heat flow. Direct methods of die measurement do however exist. In this section the three most important techniques for die temperature measurement, and their applicability to this problem are discussed. The techniques are:

- The electrical method
- The liquid crystal method
- The infra red method

7.4.1 The Electrical Method

The electrical method makes use of a temperature sensitive electrical parameter as a means of non-destructively measuring the temperature of a semiconductor die. Oettinger[58] originally used such a technique to obtain the junction temperature of a power bipolar transistor. Similarly Blackburn [59] and Jakopovic [60] have adopted the same technique for die temperature measurement in power MOSFET's.

Many device electrical parameters are temperature sensitive. Blackburn however lists a number of criteria which should be satisfied if they are to be considered as a practical device thermometer:

- Its variation with temperature must be sufficiently large to be readily measured and to provide sufficient resolution.

- The parameter must be monotonic and ideally vary linearly with temperature.

- The parameter should be stable and repeatable at least for the duration of the measurement.

- The temperature sensitive parameter should be a device parameter that is easily and quickly measured with the minimum of interference from other device parameters.

The three temperature sensitive parameters of a power MOSFET which most match these criteria are the drain source saturated on resistance ($R_{DS(on)}$), the drain source diode forward conduction voltage and the gate source threshold voltage (V_T).

7.4.1.1 Saturated On Resistance

The $R_{DS(on)}$ of a MOSFET increases exponentially with junction temperature [61]. As such, if one simultaneously measures the drain source current and voltage it is possible to determine the value of $R_{DS(on)}$ and so extrapolate the present die temperature (this assumes the initial starting temperature and corresponding value of $R_{DS(on)}$ were known). For accurate measurement however, Blackburn[59] recommends that the value $R_{DS(on)}$ be measured by virtue of a constant current supply which can be momentarily switched in after the MOSFET die has been subjected to a larger heating current.

Figure 7.2 details the measuring circuit suggested by Blackburn:

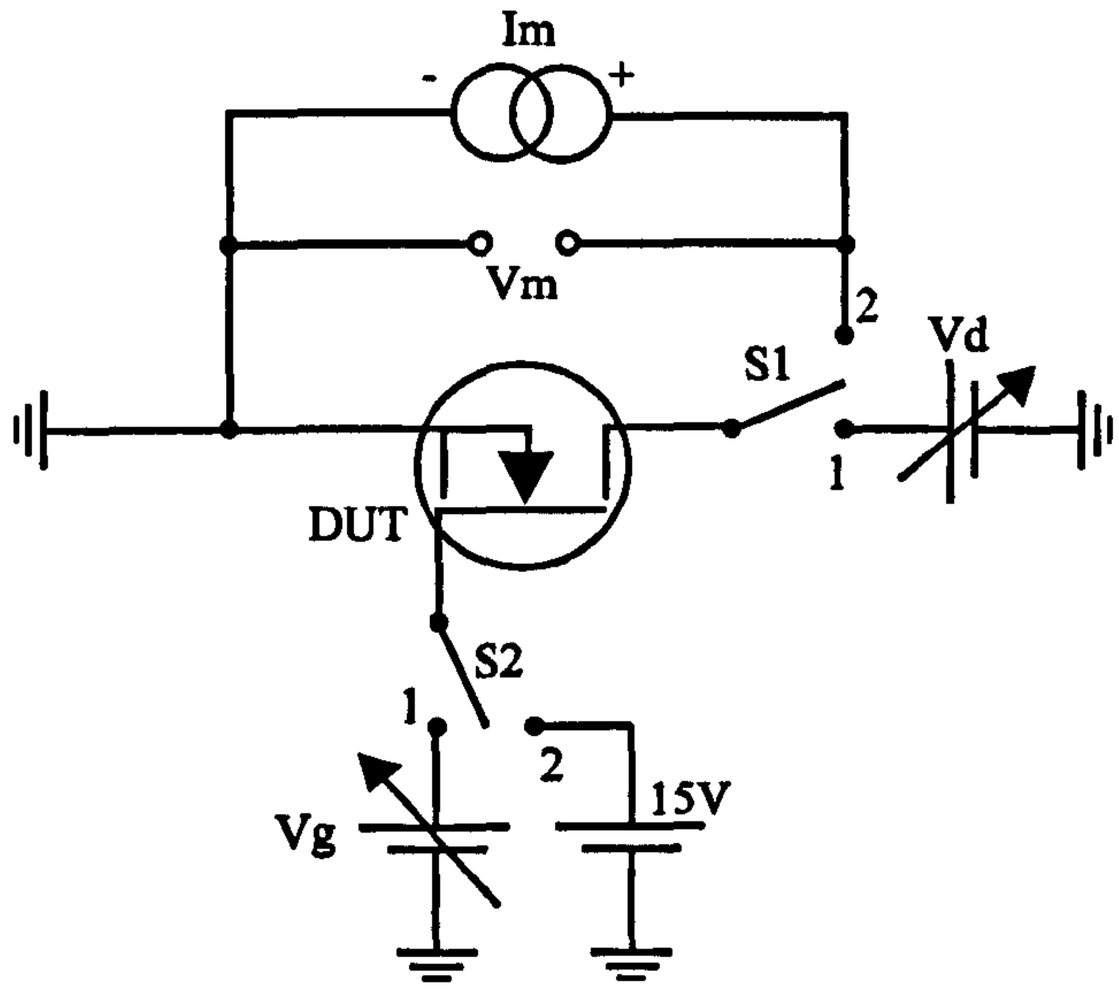


Figure 7.2 Suggested Circuit for Measuring Value of $R_{DS(on)}$

During the heating phase of the measurement, switches S1 and S2 are in Position 1 and *Vd* and *Vg* are adjusted to achieve the desired I_D and V_{DS}. To measure temperature, both S1 and S2 are switched to Position 2 and the value of *Vm* (i.e. voltage drop across the drain, source of the MOSFET) measured.

7.4.1.2 Forward Voltage of Source Drain Diode

The drain source parasitic body diode is formed as part of the MOSFET structure and is the reason why a MOSFET will not block a reverse voltage between its drain and source terminals. The forward voltage drop of this body diode can be directly sensed to indicate the temperature in the immediate vicinity of the diode. The temperature coefficient associated with the diode is such that the forward voltage drop will change typically by -2.2mV/Degrees C [62]. Under normal device operation the diode is reverse biased, and as such, it is again necessary to devise a scheme whereby a measuring configuration is momentarily switched in after a heating phase.

Blackburn suggests the circuit shown in Figure 7.3. During the heating phase switches S1 and S2 are in Position 1. The values of *Vg* and *Vd* are adjusted to achieve the desired values of I_D and V_{DS} for the heating condition. To measure temperature switches S1 and S2 are each switched to Position 2 and the parasitic diode forward voltage drop *Vm* measured.

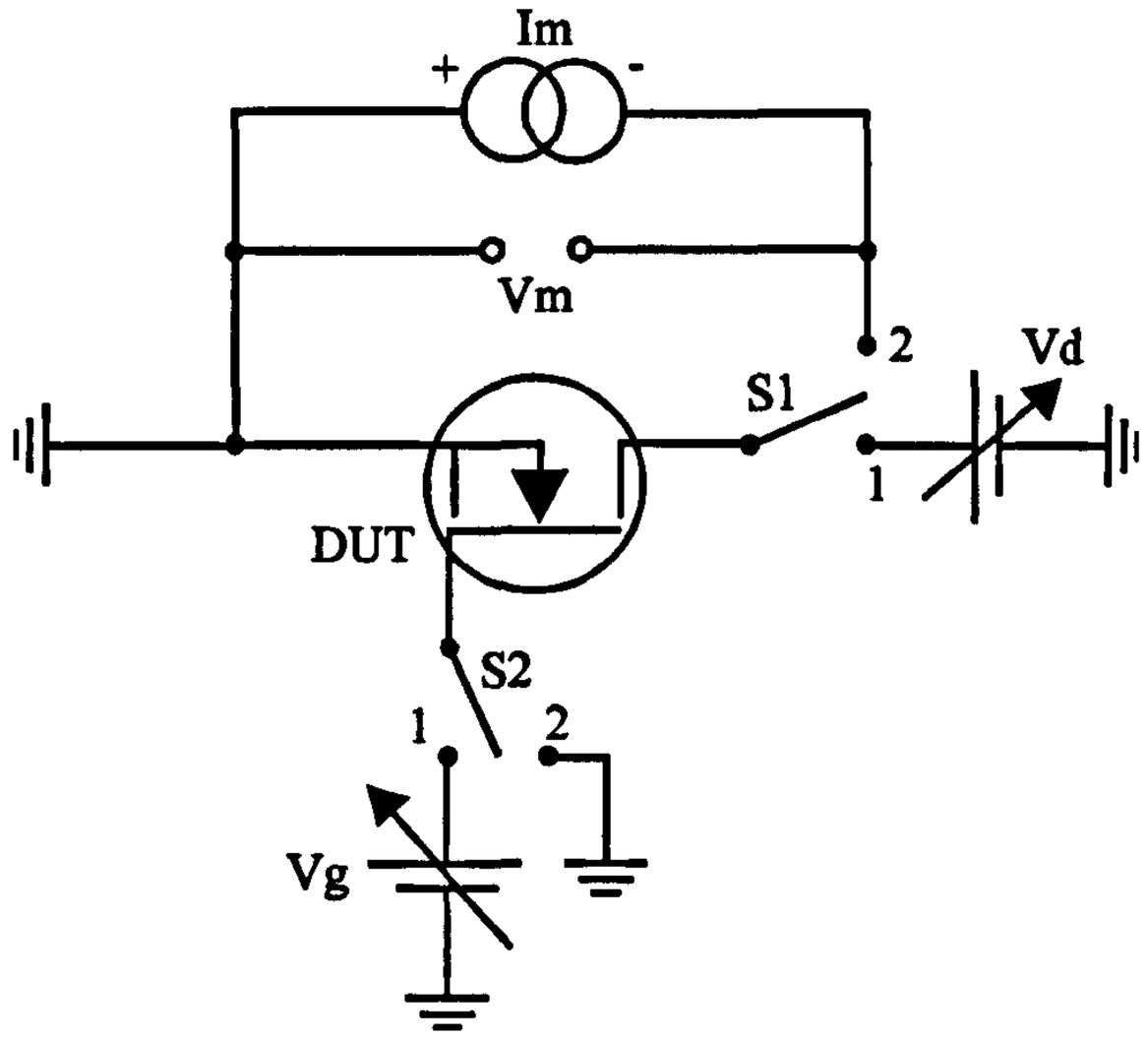


Figure 7.3 Suggested Circuit for Measuring Voltage of Drain Source Diode

7.4.1.3 Gate Source Threshold Voltage

The gate source voltage (V_{gs}) controls the on-off state of the MOSFET. The threshold voltage V_T, is approximately equal to the value of V_{gs} required to begin to turn on the MOSFET. When V_{gs} is used as a thermometer the device is only just turned on and as a consequence the value of $V_{gs} \approx V_T$. For practical devices the change in the value of V_T with temperature is approximately -2 to -6mV / Deg C. Blackburn once again suggests a test circuit shown in Figure 7.4 for measuring this parameter.

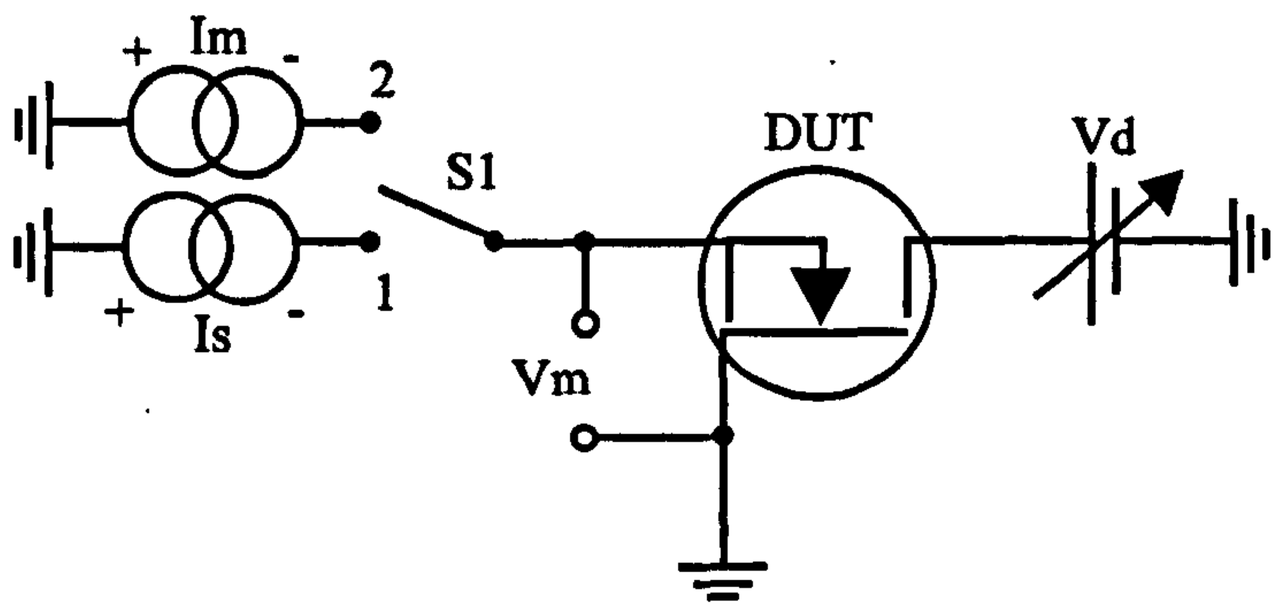


Figure 7.4 Suggested Circuit for Measuring Gate Source Voltage

During the heating phase S1 is in Position 1. The drain current is equal to *Is* and the drain source voltage is equal to *Vd*. To measure the temperature, S1 is momentarily switched to Position 2 changing the drain current to I_m, where I_m is in the range 1mA to 10 mA. During this measurement phase *Vm* can be monitored thus indicating the die temperature.

7.4.2 Cholestric and Nematic Liquid Crystal Measurement Method

7.4.2.1 Cholestric Liquid Crystals

This technique exploits the optical properties of Cholesteric Liquid Crystals. A cholesteric phase is an intermediate state between a three dimensional crystal and a liquid. The cholesteric phase is associated with a scattering affect that gives rise to iridescent colours, the dominant wavelength of which is influenced by small changes in temperature. It is feasible that if a thin layer of cholesteric liquid crystal is applied to the surface of a MOSFET die, the temperature of the die will result in a colour distribution which with careful calibration procedures could be used to obtain the surface temperature. For this technique to be applied however, certain conditions must be fulfilled [63]:

- The heat capacity of the device should be greater than the cholesteric liquid (to fulfil this condition one should choose a very thin layer of the liquid crystal).

- The device temperature should remain within the range 0 to 100 Degrees C. Outside this temperature most practical liquid crystals are not in the cholesteric phase.

- The direct use of chlorestic liquid crystal requires coating the device under test with a oil resistant agent.

- In order to absorb non-scattered light the device under test should be covered with a black coating.

7.4.2.2 Nematic Liquid Crystals

Nematogen are commonly used for their field sensitive structural change in alphanumeric displays. Their change in optical state with temperature however, can be

useful in the study of temperature limits in electronic devices. A nematic state is the state of nematogen with a particular temperature range. Below the lower threshold temperature the liquid solidifies into crystals and above the higher threshold temperature the crystals turn into an isotropic liquid.

If applied directly to the surface of the device under test as a thin film and illuminated with polarised light, liquid crystals which are above their threshold temperature may be revealed as dark patches with a minimum spot resolution of about 5 μm when the reflected light from the test area is observed with a cross analyser. Such a technique has reportedly been used to study hotspots in micro-circuits by both Stephens [64] and Macksey [65]. Nematogen have a practical upper temperature limit of 300 Degrees C and temperature sensitivities are available to a 0.5 Degrees C resolution.

7.4.3 Infrared Measurement Technique

The Infrared (IR) measurement technique is based on the detection of Infrared electro-magnetic waves emitted by a radiating body. The amount of radiated energy is related to the body temperature (as has been discussed in Section 7.2). A typical IR measurement system is shown in Figure 7.5.

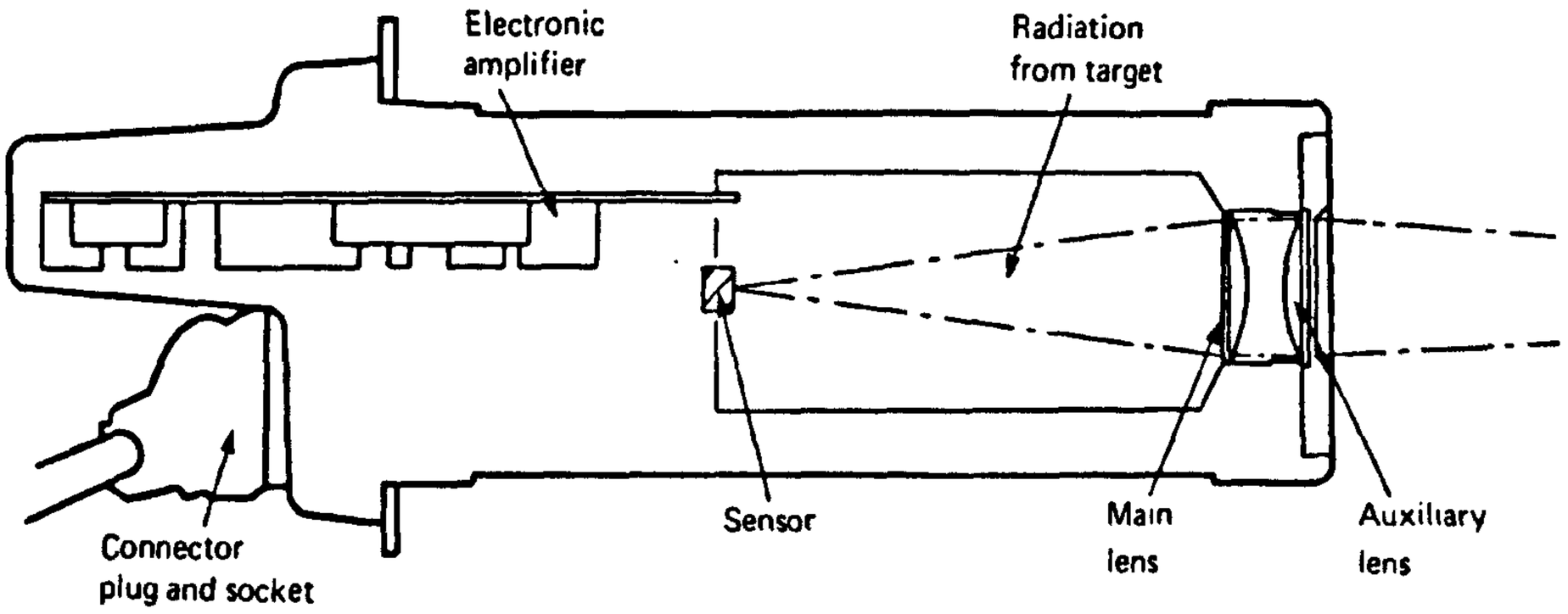


Figure 7.5 Infrared Thermal Imaging Camera

A liquid nitrogen cooled infrared detector collects the infrared waves radiated from the object under investigation. The magnitude of the collected radiation determines the amplitude of the output electrical signal which can then be amplified and processed. With this technique a temperature resolution better than 0.5 Degrees C may be achieved [66]. The technique also has an advantage in that the time constant of the detector can be as small as 1μs thus facilitating measurement of semiconductor die heating under transient conditions. Several authors have successfully applied this technique for the measurement of electrical circuits and devices (Griffin[67], Webb[68], Tian[69]). However, if the surface of the material has a very low emissivity (less than about 0.05) measurements are not possible (emmisivity is a function of the test specimen material, temperature and the IR detector). Also as the emmisivity reduces the measurements can become increasingly inaccurate unless special processing of the measurement data is undertaken. Problems of low emmsivity can sometimes be overcome by coating the device with a thin, high emmisivity, non-conducting layer which will not change its thermal distribution to any degree.

7.5 Assessment of Temperature Measurement Method Suitability

As has been stated by Oettinger [58], the ideal technique should be:

- Non-destructive
- Precise
- Easy to perform

All the temperature measurement techniques discussed so far are non-destructive. Therefore, the main issues of the comparison are suitability to the test results sought, accuracy and ease of performance.

The electrical method of determining die temperature has an advantage over the other methods in that it does not require physical or optical access to the MOSFET die in order to take temperature measurements. This means a commercially packaged Power MOSFET other than an 'open can' TO3 may be used as the test subject. Of the three parameters Blackburn [59] reports the gate source voltage V_{gs} to be the most accurate, producing results between 95% and 100% of the die temperature determined using a infrared thermal imaging camera as an accurate reference. Both the drain source body diode and the $R_{DS\ (on)}$ parameters produced temperature values with accuracy's in the range of 80% to 90% of the infrared result.

All three parameters give only an average die temperature and will not identify any temperature distribution across the die. Likewise the electrical method is considered only to be applicable for recording steady state temperatures given the requirement to momentarily switch in the measuring circuit. Such switching could give rise to many recording errors highlighted by Blackburn, these include non-thermal switching transients, significant device cooling during the measurement phase and reduced power dissipation due to lead inductance and skin effect. Arguably the value of $R_{DS\ (on)}$ could be measured continuously to record transient heating; however in order for the measurement to be representative relatively large levels of power dissipation are needed in the die to generate the desired heating. This requirement is best satisfied by placing the MOSFET into a linear mode of operation, consequently switching to a measurement configuration would still be required.

Cholesteric liquid crystal measurement is not easy to perform as it requires a careful and lengthy calibration procedure and is unsuitable for temperature measurements above 100 Degrees C. The transient time constant of cholestric liquids are about 0.1 sec which is significantly longer than the time constant of the MOSFET die (0.003 sec). As such, even if a technique could be devised to record the colour change during transient heating the disparity in the two time constants would mean an accurate temperature profile could not be attained.

Nematic liquid crystal measurement does not require the lengthy calibration procedure of cholesteric liquid crystal measurement but the technique can only provide information about those areas which have exceeded the threshold temperature. As such recording the temperature profile during a transient rise is not possible with this method.

The infrared technique is not an easy technique. The emmisivity calibration needs to be performed carefully for accurate results and is a time consuming activity. It also needs expensive image processing facilities. It is however a reasonably accurate technique and allows temperature profiles and distributions to be recorded for both steady state and transient temperature conditions. The method also has an advantage in that it does not put any electrical constraints on the test subject, and consequently the device can be powered in exactly the same way as when it will be operated in a SSPC.

The above consideration coupled with the availability of an infrared facility led to the utilisation of this technique for the validation of numerical simulations.

7.6 Infra Red MOSFET Die Temperature Measurements

The facility used for the MOSFET die temperature measurement has been previously developed in the University of Birmingham Wolfson Laboratory by Dr. P.W. Webb. Two test configurations were used, one for steady state temperature measurement and the other for the transient temperature measurement.

7.6.1 Steady State Measurements

The steady state measurements were first performed on a candidate MOSFET (IRF044) for the reasons listed as follows:-

- To confirm the sample MOSFET was free from any defects in the die bonding which could account for a higher than normal reading.

- To serve as a means of determining the true value of the device junction to case thermal resistance (Rth_{jc})

- To assist in the construction of a thermal numerical model (this topic will be discussed later in this chapter).

The test configuration for the steady state measurements utilised an Agema Thermovision 900 XY scanning microscope based on a Cadmium Mercury Telluride (CdHgTe) liquid nitrogen cooled detector (this detector has a wavelength sensitivity of between 8μm and 12μm). It uses a suitable scanning mechanism to provide the steady state thermal images of the device under test. The horizontal and vertical scanning rates are such as to provide 16 full frames per second. A computer is dedicated to the tasks of system automation and data processing. Different objectives with different magnification power and spot size can be utilised to obtain the best possible thermal images.

In order for the measured temperature to be a meaningful parameter, some well-defined reference point associated with the device must be maintained at a constant temperature during the measurement. The reference point chosen for this test is on the bottom outside of the MOSFET case directly below the semiconductor chip. The temperature is monitored at this point with a thermocouple. The device under test is firmly clasped to a temperature controlled heatsink to maintain a constant reference temperature. The heatink is made of a copper block containing both heating elements and water channels for the flow of chilled water. The heatsink temperature control is achieved by electronically controlling the power supplied to the heating elements. The flow rate of the chilled water is controlled manually by adjusting a constriction in a circulatory pump output. Owing to the fact the heatsink was electrically conducting it was necessary to electrically isolate the device from the heatsink via a thin thermally

conducting pad. Care is taken to assure the heatsink surface is flat and 'burr free'; similarly care was taken to ensure the attaching screws of the MOSFET were fastened with the same torque.

The electrical connection to the MOSFET was made via a control circuit designed and constructed specifically for this experiment. This control circuit operated the MOSFET in its linear region as a constant current source. A calibrated control was then used to select the desired level of device drain source current. The test device could be turned on and off for a precise time duration via a fast external switching input. Using such a scheme, it was possible to precisely control the level of power dissipation in the MOSFET die. Drain-source current and voltage measurement provided further assurance of the die power dissipation level. Appendix 7 presents a circuit diagram of this control circuit.

To accurately determine the temperature of the test subject using IR techniques it is necessary to calibrate the IR microscope by measuring the emmisivity of the subject. The emmisivity calibration is based on several measurements at different elevated and stabilised device temperatures (the radiation measured from any two known temperatures may be compared to those expected from a black body and used to calculate the surface emissivity).

The emmisivity of the MOSFET die was uniformly measured at 0.45 over the top surface. The exception to this was the source pad which produced a much lower reading of 0.042 owing to the lack of a silox coating. Figure 7.6-A shows the colour thermal contour map measurements produced with the Agema IR scanning microscope in which the IRF044 MOSFET die has a steady state power dissipation of 56W and a stable base temperature of 47 Degrees C. Figure 7.6-B details a similar map but with a slightly higher base temperature of 50.2 Degrees C.

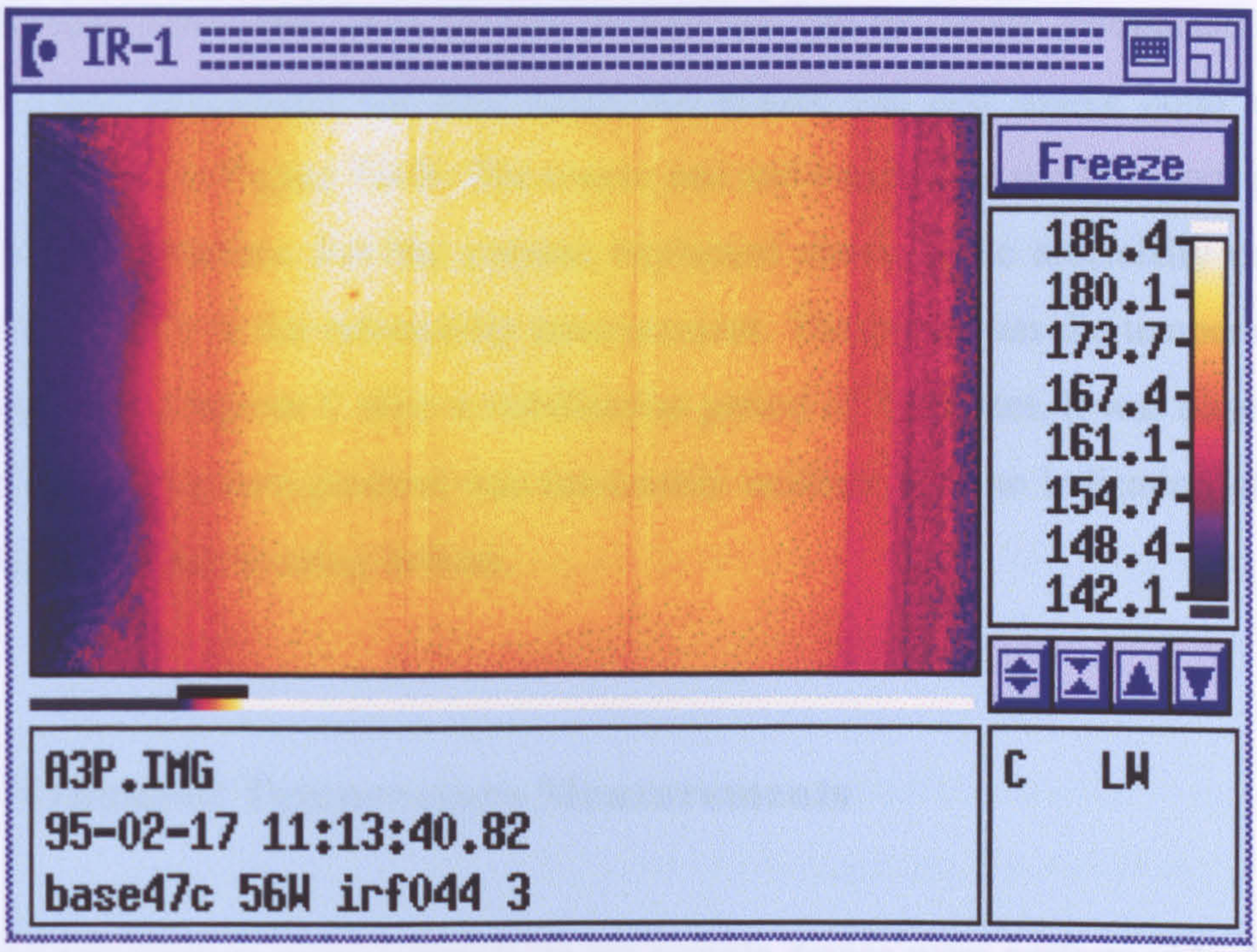


Figure 7.6-A Thermal Contour Measurement of an IRF054 at 56W Dissipation

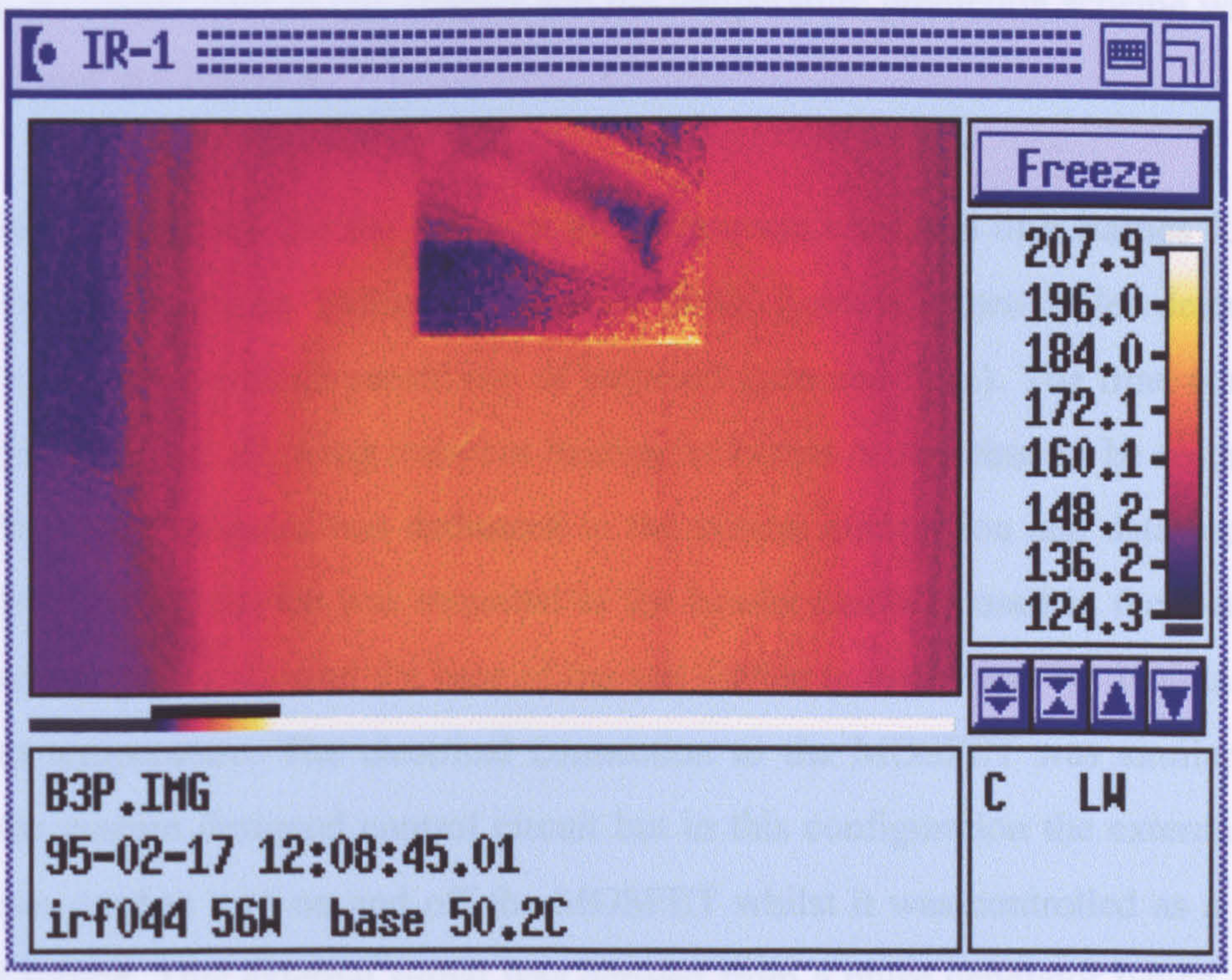


Figure 7.6-B Thermal Contour Measurement of an IRF054 at 56W Dissipation

From Figures 7.6-A and 7.6-B the device structure can be clearly recognised from the thermal plots, particularly the area where the source pad and source bond wires are placed as shown in Figure 7.6-B. The source pad and bond wires produce cool pathways in the device structure. For the reasons explained above, these artificially cool areas represent an error in the emmisivity measurement. The maximum die temperature was recorded at 186 Degrees C after a stabilisation period of 7 minutes. It was observed that the surface temperature gradient was reasonably uniform with no indication of any hot spots caused by die bonding defects.

7.6.2 Transient Temperature Measurements

Transient temperature measurements on the sample device were performed to determine how the temperature of the device changed with time for a given change in dissipated power. Such information would then be used to validate both the computer modelling activity discussed later in this chapter and the temperature prediction scheme which will be discussed in Chapter 8.

The test configuration for the transient measurements consisted of a Barnes RM2 spot microscope based on an Indium Antimonide (InSb) liquid nitrogen cooled detector (this detector has a wavelength sensitivity of between 1μm and 5μm). The time constant of this detector is 1μs allowing transient heating in excess of this time to be recorded. An IBM Personal Computer was dedicated to the system automation and data processing. The same IRF044 device was mounted to the header platform used in the steady state measurements; this allowed the base of the test device to once more be maintained at a constant temperature. The electrical connection to the MOSFET was similarly made using the custom designed control circuit but in this configuration the external control input was used to turn on and off the MOSFET whilst it was controlled as a constant current source. This external signal was derived from a pulse generator which could be programmed to output finite length switching pulses. The triggering of this pulse generator was then controlled via the PC. With suitable adjustment of the current setting

it was possible to subject the device to a finite level of dissipation for a controlled time period. As the levels of current conducted through the MOSFET die were relatively high (in the tests the current demand ranged from 17A to 70A), it was necessary to implement this requirement on a pulse basis by connecting a 80,000 μF capacitor bank between the MOSFET drain and source.

The precise level of power dissipated in the MOSFET die during each test was calculated by recording the values of drain source current and voltage on a digital storage oscilloscope and then calculating the product. It was again necessary to calibrate the IR microscope by measuring the emmisivity of the test subject. The previously recorded emmisivity value could not be used in this experiment owing to the fact each of the IR measuring devices have a different wavelength sensitivity. Using a common emmisivity reading will give rise to measurement errors despite the fact they are both recording the same test subject. The emmisivity of the test MOSFET using the Barnes Microscope was recorded at 0.16. Figure 7.7 shows an example of the temperature rise measured in the IRF044 die using this test configuration for a dissipated power level of 1000W.

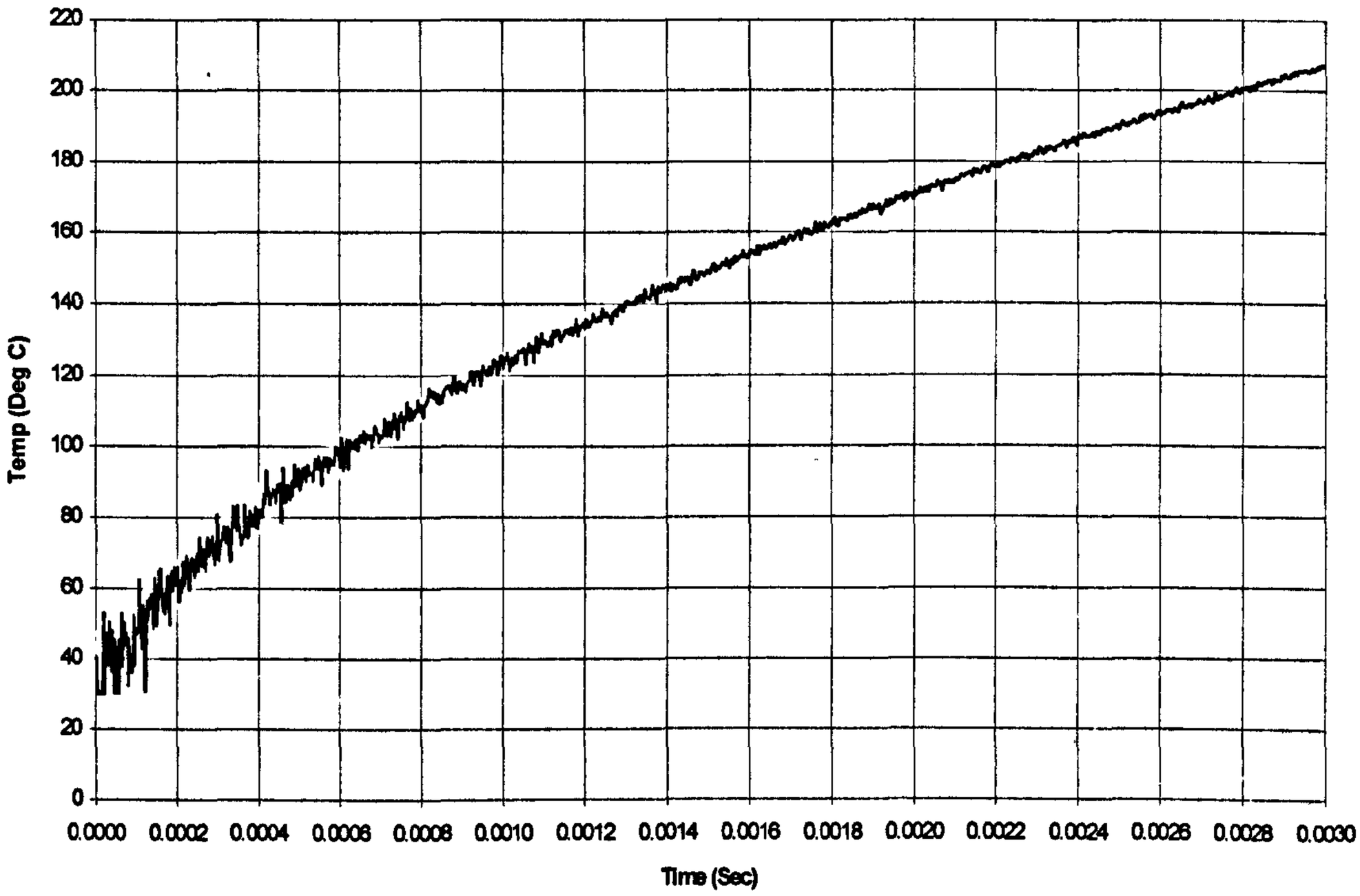


Figure 7.7 Transient Temperature Rise in MOSFET Die

From the trace it can be observed that there is a small degree of switching noise introduced into the start of the temperature rise from the constant current control circuitry. Transient temperature profiles for other levels of dissipated power were also recorded using this scheme and these will be presented later in the chapter.

7.7 Determination of Die Temperature Rise by Simulation

In the previous section it has been described how by using IR techniques it was possible to take MOSFET die temperature measurements under steady state and transient power conditions. Although these measurements yielded important results it was considered necessary to provide additional die temperature information using a computer based simulator. The reasons for simulating die heating on a computer modelling tool were:

- To determine die heating profiles for a wide variety of ambient temperature conditions and levels of dissipated power. Performing a relatively large number of measurements using an IR camera would have been impractical owing to the lengthy and time consuming nature of the technique.

- To increase confidence in the validity of the IR temperature measurements.

- To determine die temperature profiles for devices types whose package prevents the use of IR measurement techniques (i.e. plastic encapsulated TO247 or TO3P package types).

An ideal thermal simulator should provide accurate results which closely match the experimental characteristics of the device under study. A commercial Power MOSFET is a relatively complicated structure and faithful prediction of experimental results require:

- Precise details of both the Power MOSFET die and surrounding package.

- Accurate knowledge of materials used in the Power MOSFET construction.

- Knowledge of the physical properties associated with those materials.

7.7.1 Dimensional Details

The manufacturer of the Power MOSFET's used in the temperature study, provide precise details in their catalogue [35] of the size and thickness of the semiconductor die. Unfortunately no information is given regarding other details needed to construct an accurate thermal model. Such items include:- die surface metalisation thickness, die bond thickness, heat-spreader dimensions and base dimensions. To obtain these parameters it was necessary to section the test devices and physically measure the items

of interest. Sectioning a test device required encapsulating it in a plastic resin and then grinding part of it away using a fine diamond abrasive disk.

Figure 7.8 shows an example of two such devices which have been sectioned in the manner described.

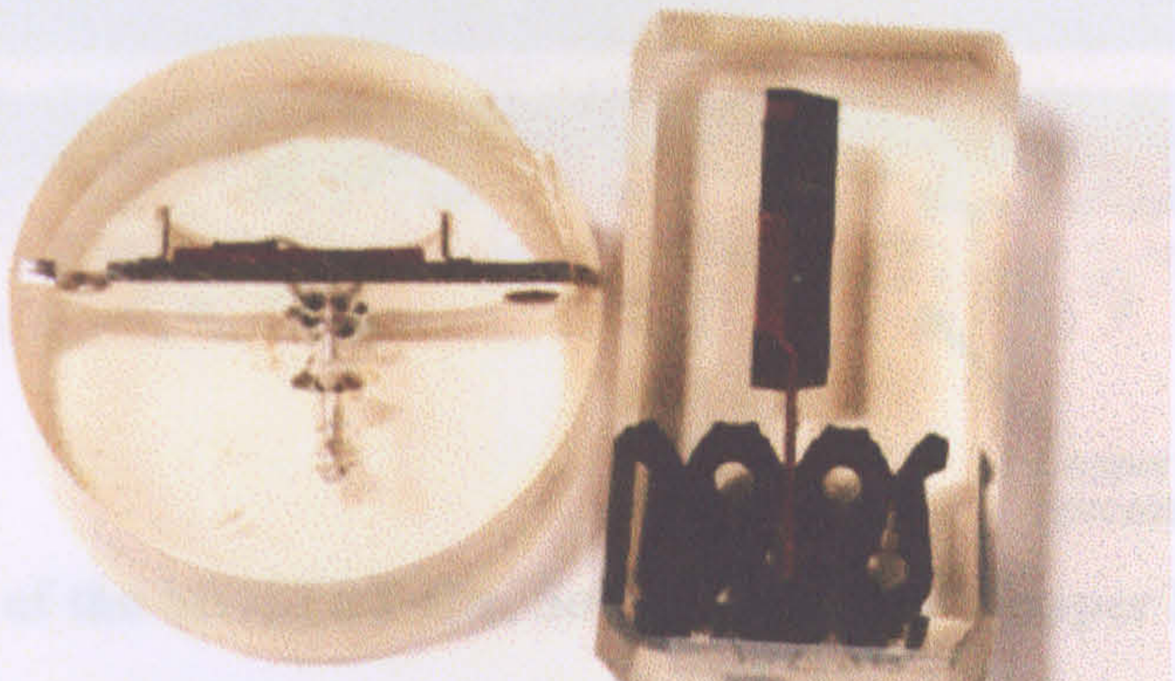


Figure 7.8 Photograph of Two Sectioned Power MOSFET's

Once sectioned to the required depth it was possible to precisely measure the parameters using an optical microscope incorporating a special measuring utility.

Figure 7.9 shows such a view of the die, indicating the die bond thickness and its uniformity in relation to the die itself. Likewise, Figure 7.10 shows an example photograph detailing the device structure at the top portion of the die. From the photograph the polysilicon gate connection, the silicon oxide layer and the die metalisation layer can all clearly be seen.

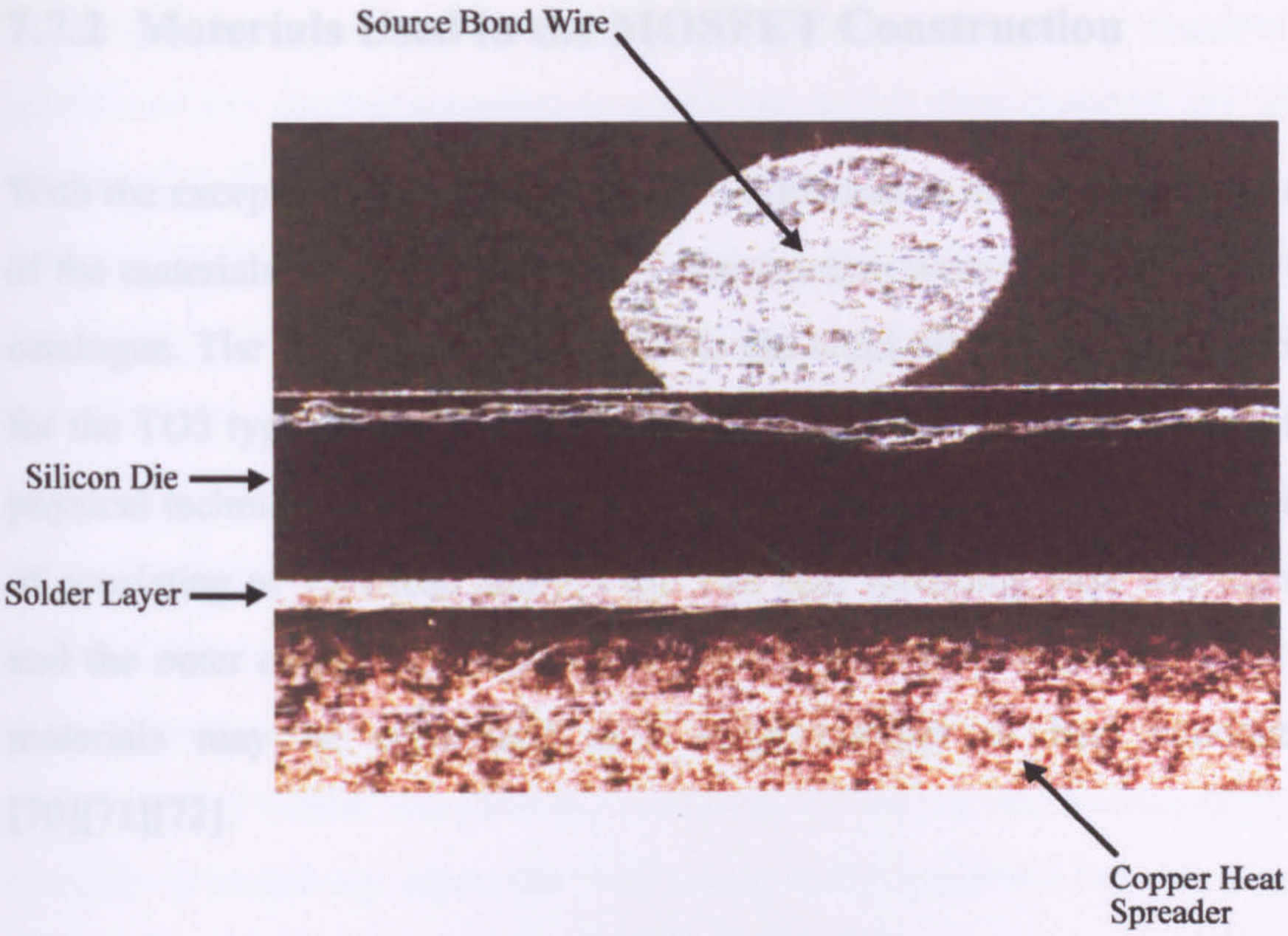


Figure 7.9 View of the MOSFET Die, Solder Bond and Copper Heat Spreader

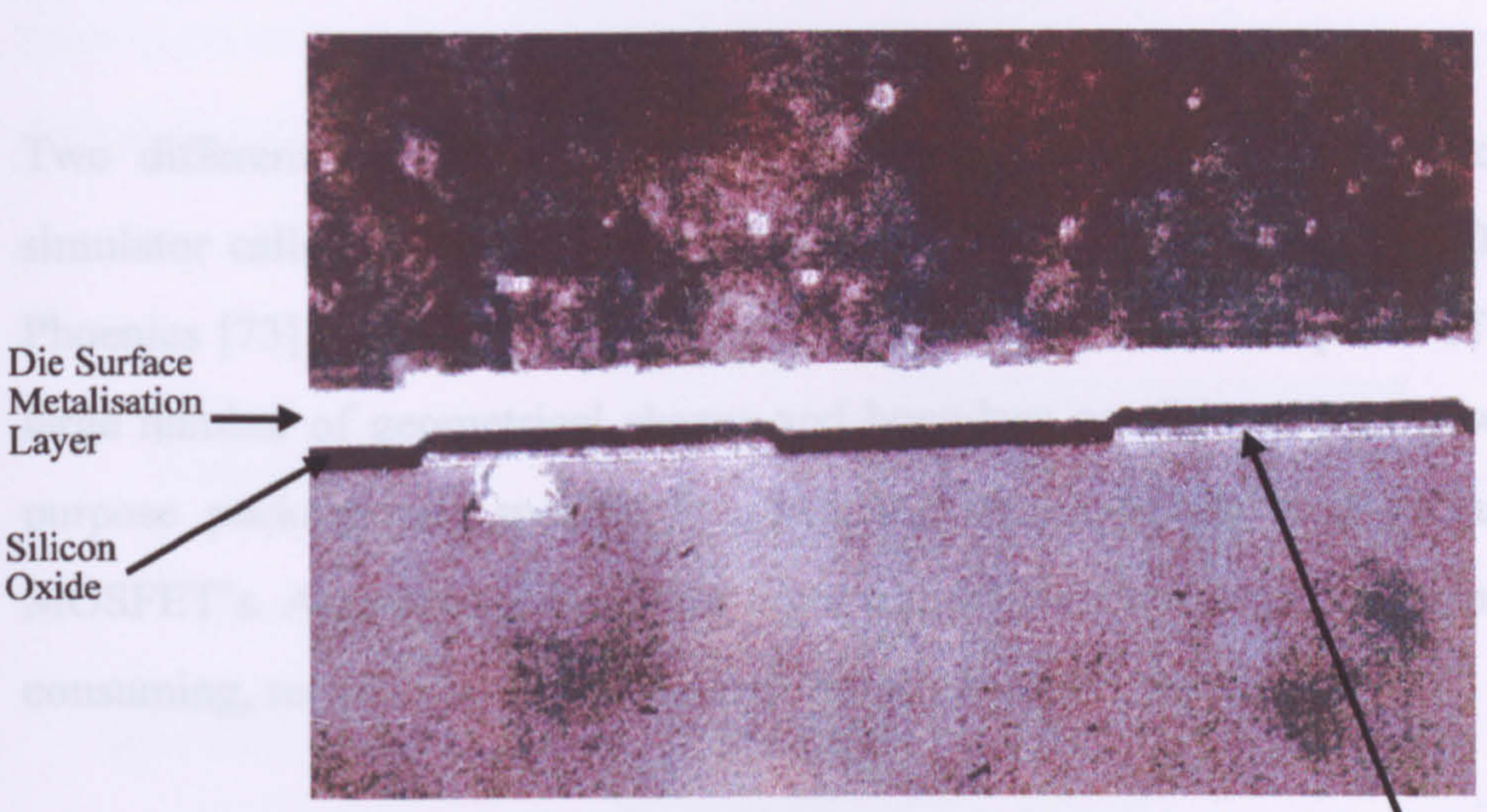


Figure 7.10 Photograph of the Device Structure at the Top of the Die

A total of 40 test devices (20 IRF044 and 20 IRF054) derived from 3 differing batches, were sectioned in order to assess uniformity and variations in the measured parameters. It was found that the items of interest were very tightly controlled by the device manufacturer and consequently any variation was too small to be of any significance.

7.7.2 Materials Used in the MOSFET Construction

With the exception of the Silicon die and Aluminium metalisation layer explicit details of the materials used in the MOSFET construction were absent from the manufacturer's catalogue. The items of interest were the die bond material, the heat-spreader/base and for the TO3 type package the metal outer casing. Using a combination of chemical and physical techniques the die bond material was ascertained to be a soft solder compound of consisting of 95% lead and 5% tin. The heat spreading base was high purity copper and the outer casing was mild steel. The physical properties associated with all these materials may be referenced in a large number of heat conduction textbooks [70][71][72].

7.7.3 Simulation of MOSFET die heating

Two different simulators were considered for this task, a commercially available simulator called Phoenics, and a proprietary simulator developed by Dr. P.W. Webb. Phoenics [73] is based on the Finite Element method and is capable of dealing with a large number of geometrical shapes and boundary conditions. It is however a general purpose package not specifically designed for modelling heat diffusion in Power MOSFET's. As a consequence, the input file can become large and its preparation time consuming, requiring a large degree of familiarity with the tool.

The proprietary simulator uses the Transmission Line Matrix diffusion modelling technique (TLM) [74] for transient simulations and the finite difference method for steady state simulation. The main purpose of the proprietary simulator is the simulation of heat transfer in electronic devices or integrated circuits. As such, the input file is greatly simplified and requires little familiarity with the simulator. It also contains an impressive post processing facility assisting in the task of assimilating the data. For these reasons the proprietary simulator was chosen in preference to its commercial counterpart.

In order to reduce processing time the proprietary simulator requires that only one quarter of the device structure is modelled as all four quarters are identical. It also divides the device structure into several main sub-blocks within which the thermal conductivity is considered to be uniform or a function of temperature. Each distinct device layer is entered in terms of its material properties (conductivity, density and specific heat capacity) and its dimensional size in all three axes. One uncertainty concerning the model was the effective area of the device base, given the copper and steel structures are irregular in shape and heat will flow both vertically and laterally within their volume. This question was solved by using the steady state infrared thermal measurement results. Using a simulated die power dissipation and reference temperature (water cooled header temperature) matching that of the real measured parameters, it was possible to iteratively adjust the dimensions of the modelled base until the simulated die temperature closely agreed with that of the measured value. Figure 7.11 details a schematic of the device structure entered into the simulator (note the heat dissipating layer is positioned directly beneath the top surface metalisation) and Appendix 8 shows a typical format of the simulator input file.

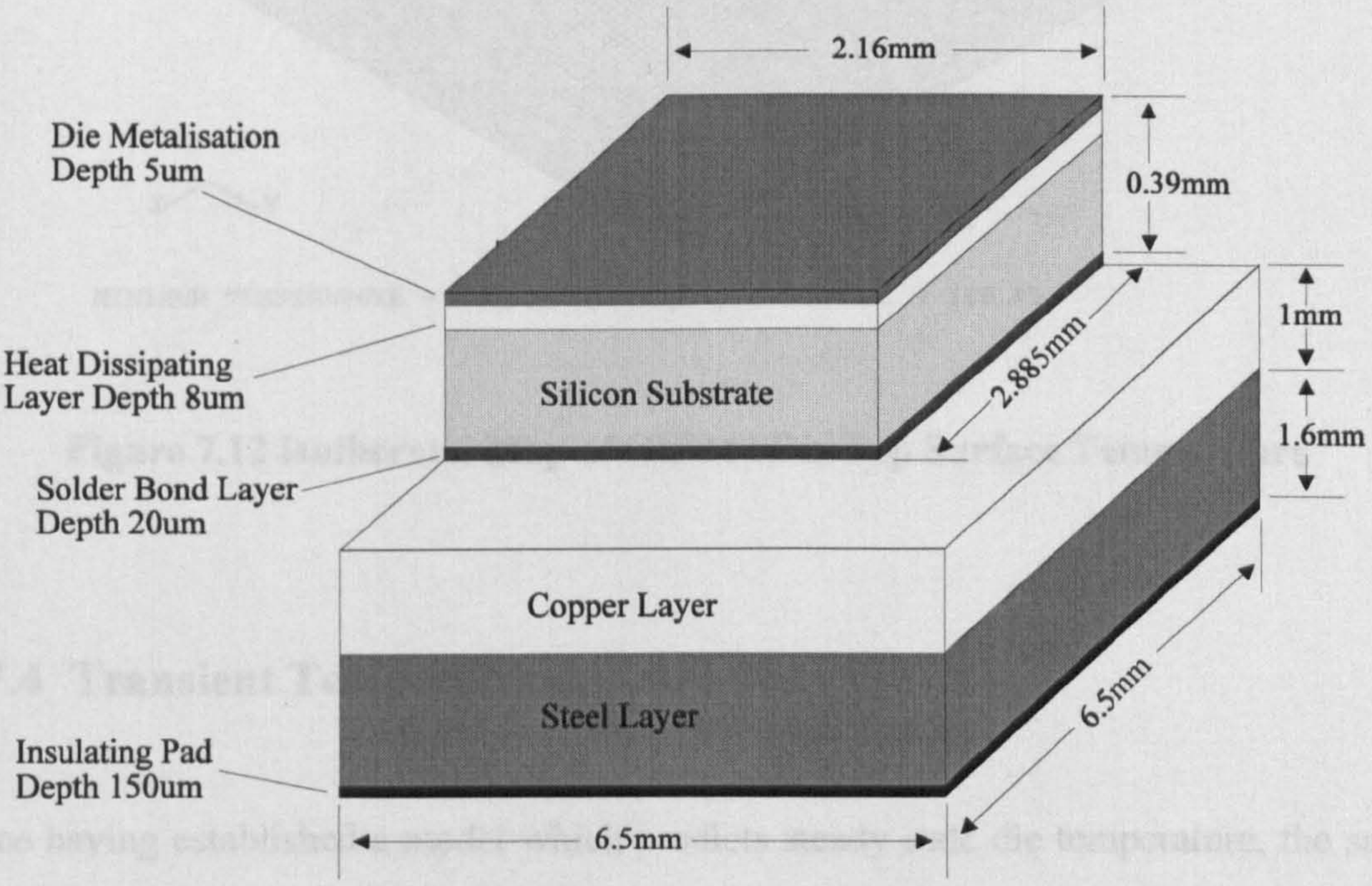


Figure 7.11 Device Structure Details Entered into Simulator

Figure 7.12 presents a thermal plot created by the steady state simulator showing the temperature distribution across the top surface of the modelled IRF044 die when steady state power dissipation is 56W. It can be observed that the modelled peak temperature is 188 Degrees C which is close to the 186 Degrees C measured under the same power conditions by the Agema IR camera.

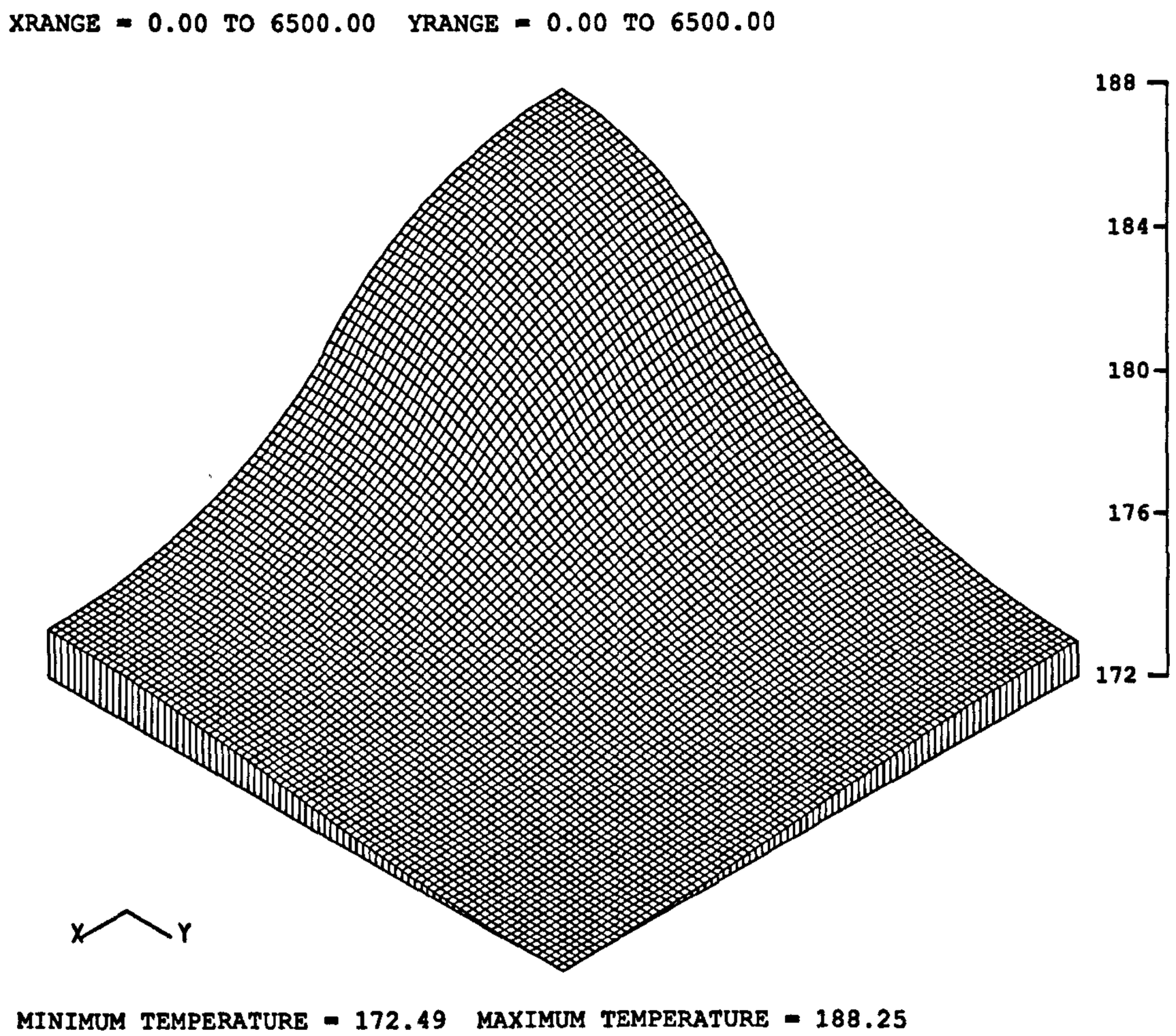


Figure 7.12 Isothermal Map of IRF044 Die Top Surface Temperature

7.7.4 Transient Temperature Simulation

Once having established a model which predicts steady state die temperature, the same model may then be used to predict die temperature under transient power conditions. The simulator can be programmed to exert a step change in dissipated power within the

modelled die. It can then predict the temperature change as a function of time. The temperature of any part of the die or device package may be examined during the time steps and a record kept of the simulated temperature. Given that the top portion of the die (the epitaxial layer) would attain the highest peak temperature under a positive power surge, attention was focused in this region.

The transient temperature profile of the IRF044 was simulated for step changes in dissipated power of between 100W and 4000W in 100W increments. Like the steady state simulations, the initial temperature of the device base was again modelled at the same temperature as the header used in the IR transient thermal measurements. Figure 7.11 presents the output of the TLM simulator for a dissipated power of 500W. In addition to the TLM output the 500W IR measured transient profile is also displayed providing an indication of the overall agreement between the measured and modelled results. Further TLM modelled temperature prediction results together with the IR recorded temperatures are displayed in Chapter 8.

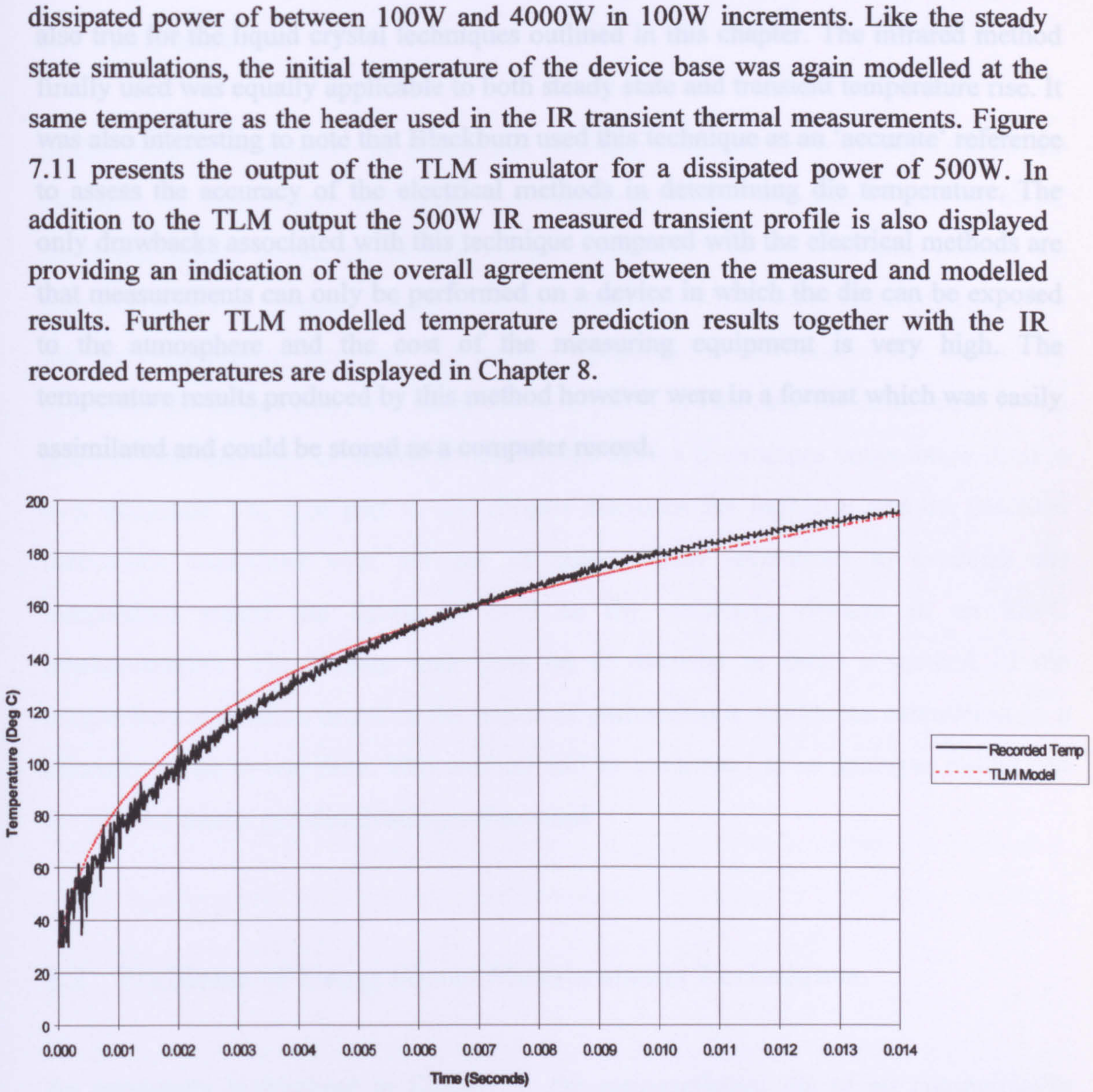


Figure 7.13 Comparison of Recorded IRF044 Die Temperature and TLM Model Temperature Prediction

7.8 Conclusions

The work detailed in this chapter has been successful in providing thermal data relating to the temperature rise in a power MOSFET, under both steady state and transient conditions. A review of electrical methods for determining die temperature concluded that electrical measurement techniques would have been problematic in relation to recording the die temperature rise under transient power conditions. This difficulty was also true for the liquid crystal techniques outlined in this chapter. The infrared method finally used was equally applicable to both steady state and transient temperature rise. It was also interesting to note that Blackburn used this technique as an 'accurate' reference to assess the accuracy of the electrical methods in determining die temperature. The only drawbacks associated with this technique compared with the electrical methods are that measurements can only be performed on a device in which the die can be exposed to the atmosphere and the cost of the measuring equipment is very high. The temperature results produced by this method however were in a format which was easily assimilated and could be stored as a computer record.

Chapter 8

Power MOSFET Die Temperature Estimation

8.1 Introduction

In this chapter we address the problem of avoiding the mode of destruction caused by excessive die temperature. In Chapter 5 it was identified that in a current limiting SSPC the power density within the die may reach levels of 500W or more for short periods. As was determined in Chapter 7, such levels of dissipation will result in rapid heating of the die and surrounding structure. To protect against MOSFET destruction caused by excessive die temperature, it is necessary to know or to calculate its temperature at any point in time and take measures to turn off the device if an upper temperature limit is ever exceeded. The first part of this chapter discusses the problems and the practical difficulties associated with the use of measurement techniques to establish die temperature whilst the device is used as the switching element in an SSPC implementation. The chapter then goes on to describe in detail a method of die temperature estimation based on the notion of performing a continuous calculation on a microcontroller in real time. This method will be contrasted to an analogue model and the relative merits and disadvantages discussed.

8.2 Problems of Using Direct Measurement Techniques

As previously highlighted in Chapter 7, the semiconductor die of all commercially packaged MOSFET's is totally encased within the package body. As a consequence, it is inaccessible to any direct temperature measuring techniques which may make use of

small measuring devices such as thermocouples or thermistors placed on, or in very close proximity to the die surface. In Chapter 7 the technique of directly gauging die temperature from the measurement of MOSFET electrical parameters was discussed. Although this technique was not utilised to record die heating it is never the less worthy of further examination as a means of determining die temperature in a SSPC implementation.

The three temperature sensitive parameters discussed in Chapter 7 were: Saturated on resistance $R_{DS(on)}$, Threshold voltage V_t and Forward voltage drop of the drain source parasitic diode.

One problem associated with $R_{DS(on)}$ is that it is not an accurate parameter and the value is liable to vary from device to device [59][61]. In order to utilise this parameter it would therefore be necessary to exercise a calibration procedure in which the $R_{DS(on)}$ value was accurately measured. Performing a calibration procedure may be acceptable for experimental temperature tests on a single device, but would certainly not be acceptable if the SSPC were to be mass produced. Similarly this variability of $R_{DS(on)}$ would complicate matters considerably if (as we will see in Chapter 9) MOSFET's are paralleled for the purposes of handling high load currents. More significant however, is the fact a MOSFET in an SSPC application may be in a linear mode of operation in order to facilitate current limiting. Under these conditions the device is no longer saturated and as a consequence the measurement of $R_{DS(on)}$ is no longer possible.

Measuring the threshold voltage V_t to determine MOSFET die temperature is dependent on the condition where the device is just turned on. Unfortunately this is not a condition associated with normal SSPC operation and is therefore not suitable.

Finally, the measurement of the forward voltage drop across the parasitic drain source body diode has a major drawback in that under normal device operation (conduction from drain to source) the diode is in a state of reverse bias. In order to place the diode into forward conduction it is necessary to turn off the MOSFET to make the

measurement. For an SSPC application, turning off the supply of power to an electrical load in order to make a die temperature measurement would almost certainly be unacceptable for many loads with electronic circuits since they require an uninterrupted supply of power in order to perform a normal operation.

In Chapter 4 devices known as 'Smart Fet's' were discussed in which a temperature sensor integrated into the MOSFET die is used to initiate a turn off sequence if a temperature threshold is exceeded. Such a scheme could feasibly be used to provide a direct output of die temperature which could then be measured by external circuitry. From a commercial perspective however, the inclusion of a die temperature sensor has many disadvantages in that the MOSFET would need to be a custom made part as no manufacturer currently provides such an 'off the shelf component' (Smart Fet's do not at present provide a temperature monitoring output). Apart from the initial development and fabrication costs one would be constrained to using a part which could not benefit from the economies of scale associated with popular readily available general purpose devices. Similarly, advances in Power MOSFET technology are consistently being made. $R_{DS(on)}$ values as low as 4mΩ are now reported for devices with current handling capabilities in excess of 30 Amperes [75]. If one were to exploit these advances in order to facilitate SSPC's with lower conduction losses it would mean developing a new custom device each time such an advancement was made. Given the practical problems associated with the techniques of direct die temperature measurement a different strategy is proposed which is based on the technique of temperature estimation.

8.3 Die Temperature Estimation

Methods which seek to predict the energy transfer which takes place between material bodies as a result of temperature difference have been the subject of study for some two hundred years [56]. Such methods seek not only to explain how heat energy may be transferred in a body, but also to predict the rate at which the exchange will take place and ultimately the temperature of the body as a function of time.

8.3.1 Solutions to the Conduction Heat Flow Problem

There are a number of techniques which exist to solve the heat flow problem. The techniques can be classified as: Graphical, Classical or Analytical, Analogue and Numerical.

8.3.2 Graphical Method

The graphical method, as the title suggests involves the use of a plotting technique (Schmidt plot) to yield an approximate temperature-time profile for simple shapes [76]. Since this method involves reading directly from a pre-generated graph it is not considered to be a method easily mechanised for semiconductor die temperature estimation given the real time constraints (temperature profiles are transient in nature) and the requirement for a totally automated solution. For this reason the graphical technique will not be explored further.

8.3.3 Classical / Analytical Method

Classical or Analytical solutions are so termed because they derive from a solution to the partial differential equation given in 7.4 subject to different boundary conditions. This approach has been the subject of much study and solutions to simple shapes are catalogued in the works of Carslaw [70], Schneider [71], Arpaci [72], Myers [77] and Ozisik [78]. Despite the immense number of analytical solutions that have been accumulated over the past 100 years, many practical applications have geometries, or boundary conditions so that an analytical solution is very complicated or has not been obtained at all. Another problem with such solutions is that they cannot normally predict temperature as a function of time when the boundary conditions are themselves varying as a function of time.

This drawback would have a direct impact on an application like an SSPC since the level of power dissipation in the die could be in a continuous state of change. Given this, together with the complexities of the die mounting arrangement (i.e. it is made up of layers of dissimilar material), the analytical solution is not considered to be a viable solution for estimating the temperature of the die in real time.

8.3.4 The Analogue Method

The analogue approach is based on the similarity between the two forms of the diffusion equation,

$$\frac{\partial^2 T}{\partial x^2} = \frac{1}{\alpha}\frac{\partial T}{\partial t} \qquad \text{- (8.1)}$$

and

$$\frac{\partial^2 V}{\partial x^2} = RC\frac{\partial V}{\partial t} \qquad \text{- (8.2)}$$

where V is the voltage, and R and C are the electrical resistance and capacitance per unit length. From a comparison of Equations (8.1) & (8.2) it is observable that the analogous quantities are voltage & temperature, current & heat flow, and electrical time constant in seconds & thermal time constant in seconds. At this point it is useful to introduce the physical quantities known as thermal resistance and thermal capacitance.

Thermal resistance, R_{th}, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat transfer (conduction, convection and radiation), is given by the equation:

$$R_{th} = \frac{\Delta T}{P} = \frac{\Delta T}{Q/\Delta t} \qquad \text{- (8.3)}$$

where ΔT is the temperature difference across the thermal path, P is the power dissipation in Watts, Q is heat in Joules and t is time in seconds.

As implied by Equation 8.3 the units of thermal resistance are Degrees C per Watt.

For a given structural element, R_{th} depends on the length and cross-sectional area of the thermal path, and the conductivity of the material through which the heat must flow. R_{th} of a structural element is thus defined as:

$$R_{th} = \frac{L}{kA} \qquad \text{- (8.4)}$$

where L is the length of the path in Meters, A is the cross sectional area of the path in meters^2 and k is the material conductivity in Watts per degrees Celsius per Meter.

Thermal capacitance, C_{th}, is a measure of a physical element's capability of accumulating heat, like a capacitor accumulates electrical charge. The general definition of thermal capacitance is given by the equation:

$$C_{th} = \frac{Q}{\Delta T} \qquad \text{- (8.5)}$$

where Q is heat in Joules and ΔT is the temperature change in Degrees C. Again as implied by Equation 8.5 the units of thermal capacitance are Joules per Degrees Celsius.

For a given structural element, C_{th} depends on the volume of the element in meters^3 , the material density and the specific heat capacity of the material. The C_{th} of a structural element is thus defined as:

$$C_{th} = VC_p\rho \qquad \text{- (8.6)}$$

where V is the volume, C_p is the specific heat capacity and ρ is the material density.

For a given configuration of device and package the electrical analogy of the thermal behaviour is a chain of RC cells, each having a characteristic time constant [56] [79]. Figure 8.1 shows a representation of the die and mounting arrangement previously detailed in Figure 7.1.

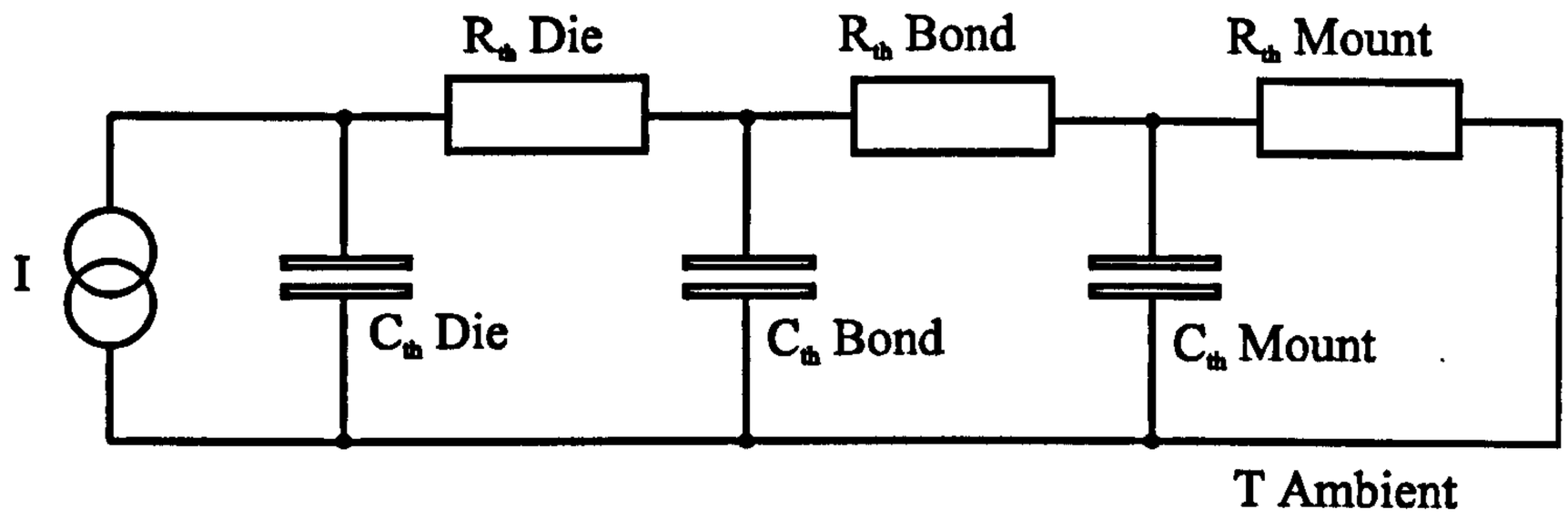


Figure 8.1 Electrical Representation of MOSFET Thermal Model

In this example each RC cell represents one of the elements of the construction. The first cell (die) represents the thermal characteristics of the silicon die itself, the second cell (bond) represents the die attach material (normally a soft solder compound) which bonds the die to the mount, and the third cell (base) represent the thermal characteristics of the mount. Assuming the device is not connected to a heatsink, following the mount heat is transferred to ambient through the effects of convection and radiation.. The current source I is proportional and representative of the power dissipated in the die structure.

As previously discussed in Section 7.1, since the heat in a Power MOSFET is dissipated in a very small area at the top of the die, it is apparent that the thermal resistance from the source of the dissipation to ambient is dependent on the thermal resistance of each of

the layers added in series (this is a quantity commonly quoted in MOSFET manufacturer's catalogues, and is referred to as the thermal resistance junction to ambient $R_{th\text{-}ja}$). Using such knowledge it is possible to calculate the die temperature by simply measuring power dissipation of the die and the ambient temperature. The temperature of the die is thus given by:

$$T_j = P_d \cdot R_{th-ja} + Ta \qquad \text{- (8.7)}$$

where T_j is the junction temperature, P_d is the power dissipation and T_a is the ambient temperature.

Equation 8.7 however, only applies when the device is in a condition of steady state and where the thermal capacitance associated with each of the layers has no further affect. In steady state the energy dissipated in the junction is equal to the energy transferred to the ambient surrounds. Under transient power conditions, the junction temperature change is also ruled by the heat accumulation in each of the cells, each following its own time constant according to the equation:

$$\Delta T = P_d \cdot R_{th} \cdot \left(1 - e^{(-t/\tau)}\right) \qquad \text{- (8.8)}$$

where ΔT is the change in the cell temperature, R_{th} is the thermal resistance of the cell, t is the time in seconds and τ is the product of R_{th} and C_{th} for that cell.

It can be seen from the above equation that each of the individual layers will be characterised by distinct thermal behaviour, dictated by its thermal time constant (τ). In most commercially packaged power MOSFET's the silicon die and the die bond layer are characterised by small volume and a corresponding low thermal capacitance. Consequently they have low values of τ, typically in the order of a few milliseconds. The mount by contrast, is normally much larger and has a correspondingly higher thermal capacitance. The value of τ associated with the mount is typically measured in

hundreds of milliseconds. These differences mean that those parts of the MOSFET with a low value of τ will change temperature more rapidly for a given change in dissipated power. For this reason it is inadequate to simply measure the temperature of the outside of the MOSFET package in order to gauge the die temperature, since the die could quickly attain a critically high temperature whilst the die mount temperature has only increased moderately.

8.3.5 Numerical Method

The numerical method of solving the temperature estimation problem involves the writing of node equations which are used to provide an approximation of the device temperature. There are a number of differing techniques which come under the umbrella of numerical methods, these include: Finite Element [80], Transmission Line Matrix [73] and Finite Difference [56].

The Finite Element method can deal with a large number of geometrical shapes and boundary conditions. For this reason it is the most commonly exploited technique in commercial simulation packages. This ability to generate a numerical mesh which aligns well with most geometrical shapes is however at the expense of extra complexity. This complexity translates into an increased time to calculate the temperature of each element in the model.

A feature of the Transmission Line Matrix method is that the numerical stability of the calculations are not dependent on the time step used in the formulation (this topic will be discussed in Section 8.3.5.2). Although this feature means that the time step can be increased beyond that which is acceptable for the other methods, an increased time step does however result in a larger error in the overall temperature prediction output. Likewise, the relaxing of the time increment constraints also translates into extra complexity in the overall method.

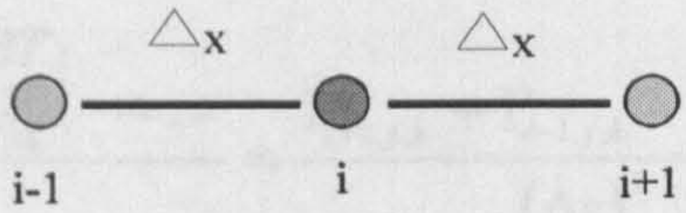
The Finite Difference method has been identified as being the simplest, and hence fastest to compute. The importance of execution speed will be discussed later in this chapter and will be discussed at length in Chapter 9. It will also be shown in Chapter 9, that it is ultimately the constraints of acceptable performance that dictate the size of the time increment (the increment required for acceptable performance has been found to be smaller than that required for numerical stability).

In view of the importance placed on fast execution time, the Finite Difference method will now be reviewed.

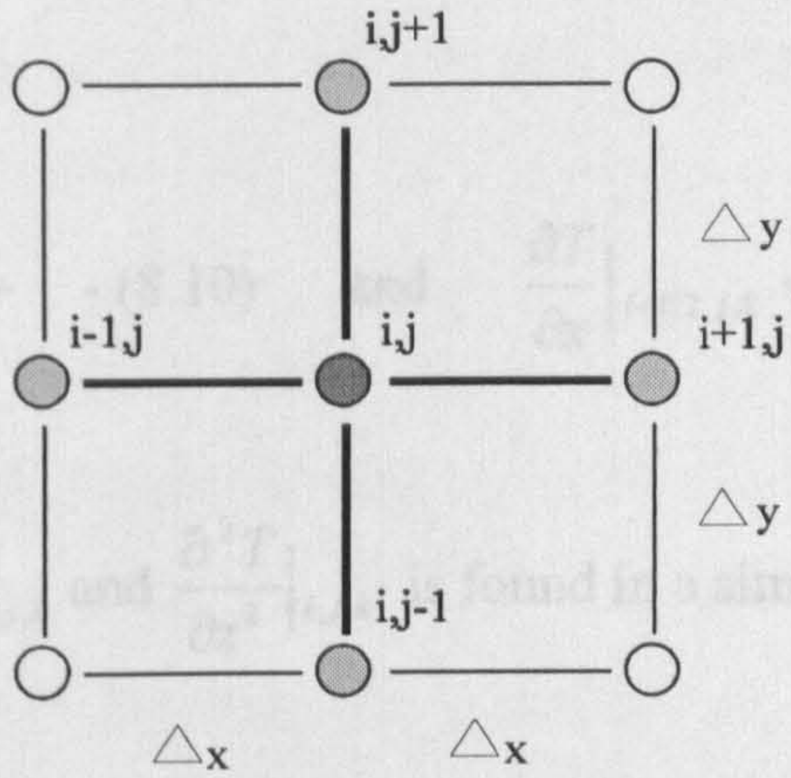
8.3.5.1 Finite Difference Method

In this technique the subject structure is divided into a grid composed of separated nodes. In a one dimensional structure each node is usually in the vicinity of two other nodes, for a two dimensional structure this increases to four and in a three dimensional structure this increases further, to six other nodes.

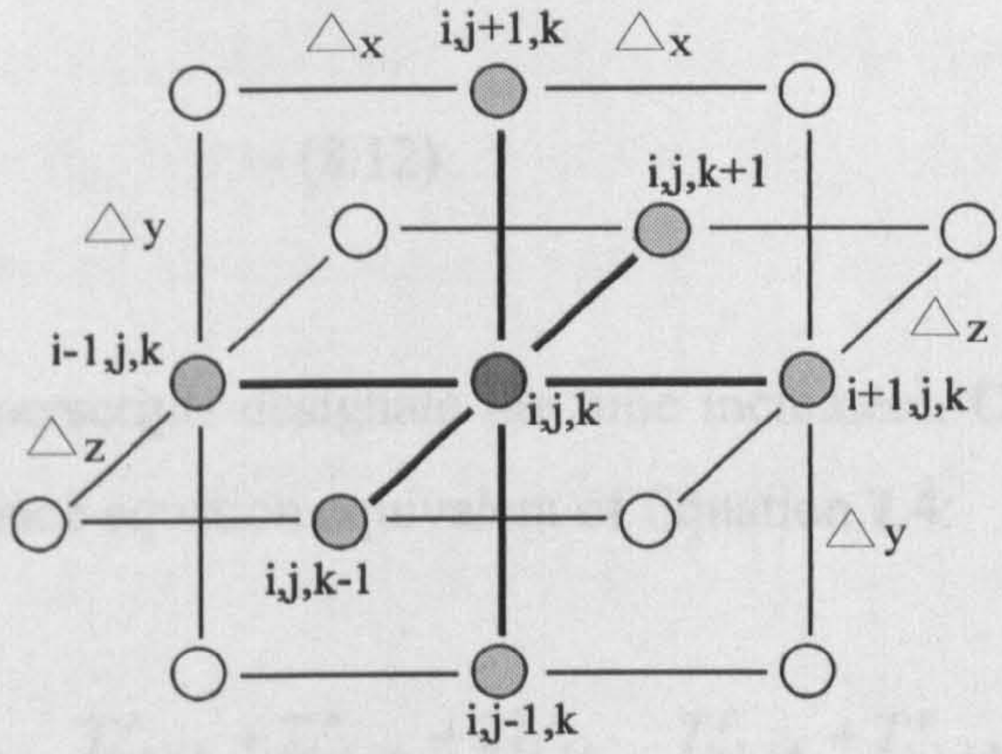
Figure 8.3 shows the typical grid topologies for the three structures.



1 Dimentional Node Structure



2 Dimentional Node Structure



3 Dimentional Node Structure

Figure 8.2 Finite Difference Grid Structures

Assuming that a finite difference mesh is devised such that the variation in temperature between any two consecutive nodes is linear and the nodes were labelled *i,j,k* according to the three dimensional structure in Figure 8.2, then the spatial variation of temperature along the x axis at node *i,j,k* can be approximated by:-

$$\left.\frac{\partial^2 T}{\partial x^2}\right|_{i,j,k} \approx \frac{\left.\frac{\partial T}{\partial x}\right|_{i+1/2,j,k} - \left.\frac{\partial T}{\partial x}\right|_{i-1/2,j,k}}{\Delta x} = \frac{T_{i+1,j,k} + T_{i-1,j,k} - 2Ti,j,k}{(\Delta x)^2} \quad \text{- (8.9)}$$

where

$$\left.\frac{\partial T}{\partial x}\right|_{i+1/2,j,k} \approx \frac{T_{i+1,j,k} - T_{i,j,k}}{\Delta x} \quad \text{- (8.10)} \quad \text{and} \quad \left.\frac{\partial T}{\partial x}\right|_{i-1/2,j,k} \approx \frac{T_{i,j,k} - T_{i-1,j,k}}{\Delta x} \quad \text{- (8.11)}$$

The approximation of $\left.\frac{\partial^2 T}{\partial y^2}\right|_{i,j,k}$ and $\left.\frac{\partial^2 T}{\partial z^2}\right|_{i,j,k}$ is found in a similar manner.

The time derivative are approximated by

$$\frac{\partial T}{\partial t} \approx \frac{T_{i,j,k}^{p+1} - T_{i,j,k}^{p}}{\Delta t} \quad \text{- (8.12)}$$

In this relation the superscripts designate the time increment. Combining the relations above gives the difference equation equivalent of Equation 7.4:

$$\frac{T_{i+1,j,k}^{p} + T_{i-1,j,k}^{p} - 2T_{i,j,k}^{p}}{(\Delta x)^2} + \frac{T_{i+1,j,k}^{p} + T_{i-1,j,k}^{p} - 2T_{i,j,k}^{p}}{(\Delta y)^2} + \frac{T_{i+1,j,k}^{p} + T_{i-1,j,k}^{p} - 2T_{i,j,k}^{p}}{(\Delta z)^2} + \frac{q}{k} = \frac{1}{\alpha}\frac{T_{i,j,k}^{p+1} - T_{i,j,k}^{p}}{\Delta t}$$

- (8.13)

If the temperatures of the various nodes are known at any particular time, the temperatures after time increment Δt may be calculated by writing an equation similar to Equation 8.13 for each node and obtaining the values of $T_{i,j,k}^{p+1}$. The procedure may be repeated to obtain the distribution after any number of time increments.

Despite the potentially large number of equation terms, modern computers can solve such problems by using either direct or iterative methods. Since the finite difference method is only an approximation of the heat flow problem clearly the smaller Δt and $\Delta x,y,z$ (i.e. the greater the number of nodes for the model subject) then the greater the model accuracy. The disadvantage associated with a large number of nodes is the increased time to calculate a result.

8.3.5.2 Finite Difference Model Using R_{th} and C_{th}

In Section 8.3.4 the analogy between the quantities of electrical resistance and capacitance and their thermal equivalents were discussed. Describing the thermal model of a semiconductor die and mount arrangement in these terms is convenient from a SSPC developer's viewpoint since information about the thermal characteristics of Power MOSFET's (i.e. R_{th} Junction to Case and R_{th} Junction to ambient) are normally conveyed in this manner by the device manufacturer.

The previous section has described how conduction problems may be solved by finite difference approximations to the differential equations. In formulating the equations however, the quantities of R_{th} and C_{th} could equally have been used for determining heat transfer between nodes.

Each volume element can be viewed as a node which is connected by thermal resistance's to its adjoining neighbours as shown in Figure 8.3.

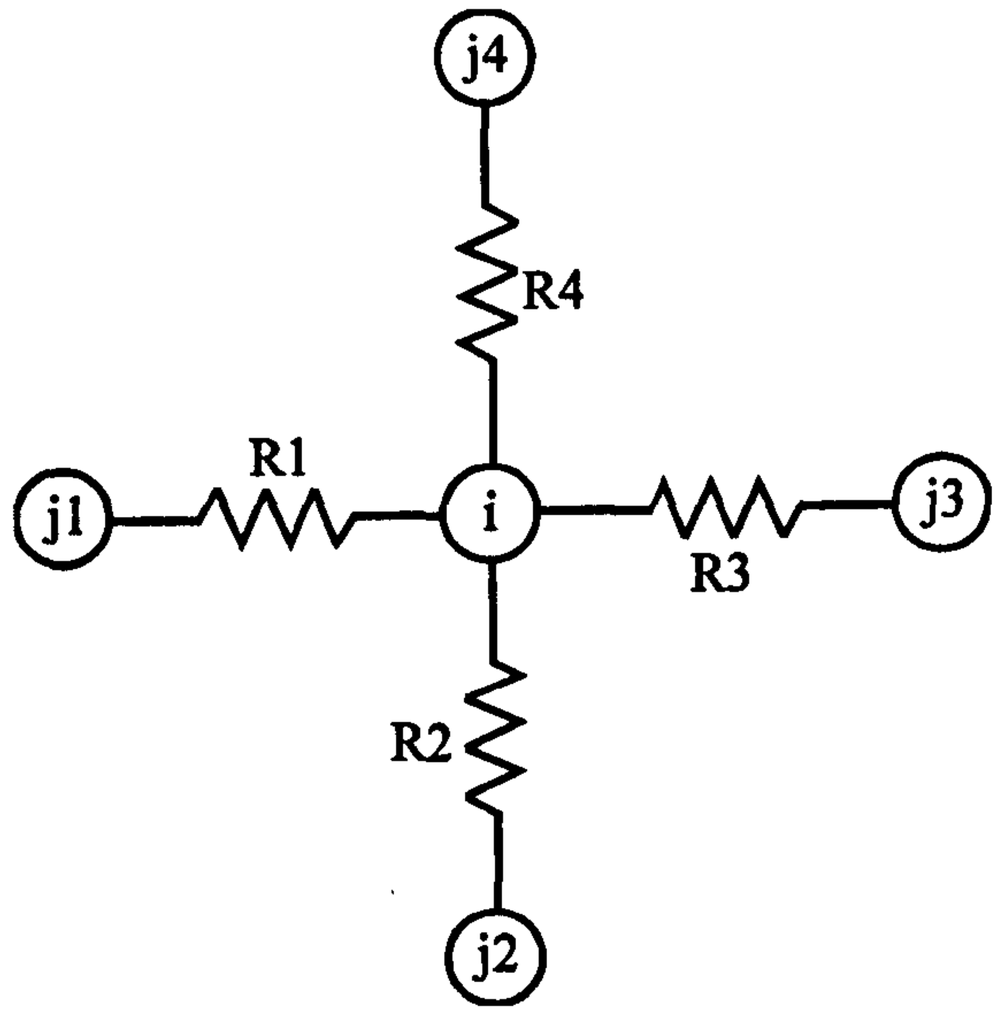


Figure 8.3 Schematic of Nodal Arrangement Joined by Respective R_{th} Values

For steady state conditions the net energy transfer into the node is zero (i.e. the power transferred into the node is the same as the power transferred out of the node). Designating our node of interest with the subscript '*i*' and the adjoining nodes with the subscript '*j*', the condition can be expressed by the following nodal equation:-

$$q_i + \sum_j \frac{T_j - T_i}{R_{ij}} = 0 \qquad \text{- (8.14)}$$

where T is the temperature of the node, q_i is the heat delivered to node *'i'* and R_{ij} is the thermal resistance between two adjoining nodes.

For transient conditions, the energy transfer results in a change in the internal energy of the element. As such, each volume element behaves like a small 'lumped capacity', and the interaction of all the elements determines the behaviour of the solid during transient conditions.

If the internal energy of the node *i* is expressed in terms of thermal capacitance and temperature then its rate of change with time can be approximated by:

$$\frac{\Delta E}{\Delta t} = C_i \frac{T_i^{p+1} - T_i^p}{\Delta t} \qquad \text{- (8.15)}$$

where C_i is the value of thermal capacitance for the node i, T is the temperature and Δt is time step.

Given this the general thermal resistance-capacitive formulation for the energy balance on the node is:

$$q_i + \sum_j \frac{T_j^p - T_i^p}{R_{ij}} = C_i \frac{T_i^{p+1} - T_i^p}{\Delta t} \qquad \text{- (8.16)}$$

Equation 8.16 can now be solved to provide a term describing the predicted temperature on the node after a time increment of Δt for the given power dissipation:

$$T_i^{p+1} = \left(q_i + \sum_j \frac{T_j^p}{R_{ij}} \right) \frac{\Delta t}{C_i} + \left(1 - \frac{\Delta t}{C_i} \sum_j \frac{1}{R_{ij}} \right) T_i^p \qquad \text{- (8.17)}$$

In order that Equation 8.17 is stable T_i^p cannot be negative since if it were the equation would then violate the second law of thermodynamics i.e. heat would have to flow from a lower temperature node to a higher temperature node. The minimum stability requirement is therefore:

$$\left(1 - \frac{\Delta t}{C_i} \sum_j \frac{1}{R_{ij}} \right) \geq 0 \qquad \text{- (8.18)}$$

This requirement will determine the maximum time increment that may be used in the calculation, given the most restrictive node parameters (i.e. minimum values of R_{th} and C_{th} for a particular node).

Solving Equation 8.18 for Δt therefore gives:

$$\Delta t \leq \left[\frac{C_i}{\sum_j \left(1/R_{ij}\right)} \right]_{\min} \qquad \text{- (8.19)}$$

Global assembly of Equation 8.17 for the entire MOSFET structure will lead to a system of equations which can be solved by a direct or iterative method.

8.4 Assessment of Model Accuracy and Method Suitability

The accuracy of the thermal model is considered to be an important factor in any SSPC implementation owing to the fact that if the model predicts a silicon die temperature lower than it is in reality, then under fault conditions the MOSFET could be commanded to remain on even though the silicon die temperature has reached its maximum limit. Such a situation could ultimately lead to the MOSFET being destroyed and thus compromising the entire function of the SSPC. Similarly, if the model predicts a silicon die temperature much higher than it is in reality, this will then have the effect of lowering the overall performance of the SSPC by making it more prone to transient nuisance tripping or unable to power electrical loads with a large inrush current requirement. A model which predicts a temperature too high will also have a detrimental impact economically, since an SSPC may require more silicon area than it would otherwise need in order to satisfy the model prediction for a given power dissipation. This is will of course increase the overall cost of the SSPC.

A practical analogue implementation of modelling a heat flow problem using electrical resistors and capacitors in the manner described in Section 8.3.4 has been reported by Neveu [22]. This model was constructed using 'lumped parameters' i.e. where each of the material layers were modelled with a single RC cell. Such a model is somewhat idealised in that it assumes each part of the layer will change temperature uniformly.

The lumped parameter model as advocated by Neveu is attractive from an implementation point of view since each of the layers which make up the model are easily identifiable. Analysis performed by Newell [78] however, has shown the most accurate analogy for the heat flow in a finite length of material is a finite length of distributed RC transmission line. To construct a model consisting of a number of transmission elements would be very difficult to achieve in practice owing to the fact it is essentially an infinite number of RC networks. As a compromise, further work by Sueker [81], has reported that a representation of an object the size of a silicon die can be modelled with a reasonable degree of accuracy with just 3 RC networks. The remainder of the semiconductor packaging would of course require further RC cells to provide the full model.

The findings of Newell and Sueker would therefore suggest a larger number of RC cells are required to realise a solution with increased accuracy (this will be confirmed later in the chapter). Increasing the number of components will of course have the disadvantage of making the physical model larger. Such a problem may also be compounded owing to the fact each of the R_{th} and C_{th} values must be modelled with an electrical equivalent. It is highly probable the values of R_{th} and C_{th} are such that they will not neatly fit into the standard electrical component values and will therefore require either custom made devices which have the disadvantage of increased cost, or alternately each RC cell may be made up of a combination of values which together give the desired quantity. This solution will of course increase the physical size of the model even further. The numerical method by contrast, is neither effected by the physical size problem or the problem of realising R_{th} and C_{th} values. The numerical method is however effected in that a larger model inevitably will increase the execution time of the prediction algorithm. As will be seen later in the chapter, this places constraints on how quickly the prediction mechanism can respond to a condition which causes excessive die heating.

Apart from the issue of the number of RC cells required for the model there is another consideration which also has a direct impact on model accuracy. This relates to the fact that for most materials the physical parameters i.e. conductivity, specific heat capacity

etc., are temperature dependent. In the majority of materials this variation is relatively small i.e. less than 5% over the temperature range -40 Degrees C to 140 Degrees C. In silicon however, the value of conductivity changes by over 150% for the same range [45].

Figure 8.4 shows the variation of undoped silicon as a function of temperature.

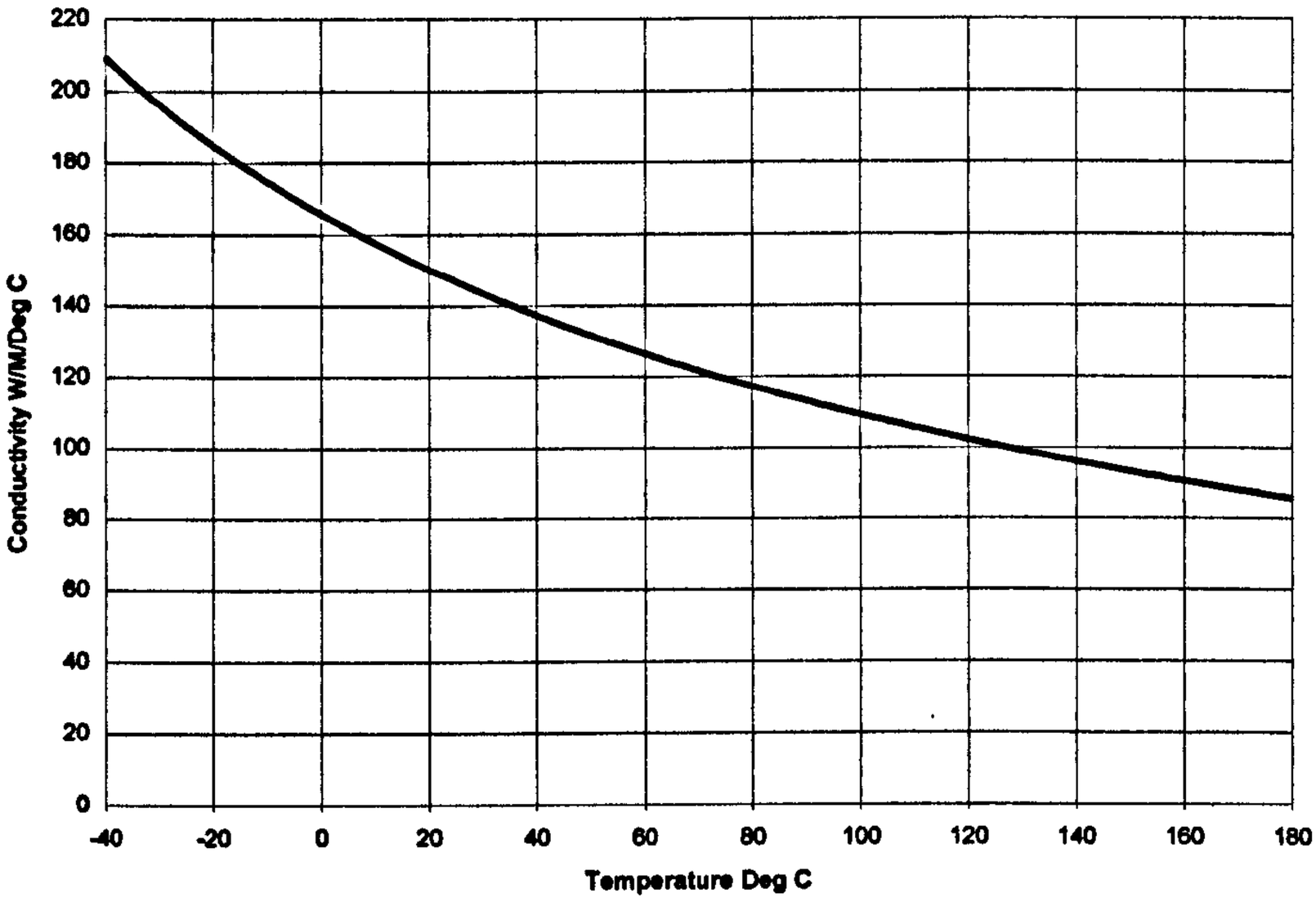


Figure 8.4 Conductivity of Undoped Silicon as a Function of Temperature

A difference such as this, if ignored, will obviously give rise to an inaccuracy in the model (the magnitude of this inaccuracy will be highlighted later in the chapter). Consequently, a thermal model consisting of simple resistors and capacitors would be unable to recreate this non-linear behaviour which occurs in reality. Once again, the numerical model has an advantage over the analogue solution in that it is possible to introduce a compensation term into the equation to take into account this conductivity change.

Equation 8.20 is an example of such an equation which can predict silicon conductivity as a function of temperature [82].

$$k = \left(\frac{32000}{T+193}\right) \qquad \text{- (8.20)}$$

where k is the value of conductivity in W/m^3/Deg C and T is temperature in Deg C.

As a final consideration surrounding the topic of model accuracy it should be noted that the complexity of the analogue circuit required to convert a measure of the power dissipated in the silicon die into a proportional value of current would not be trivial if a reasonable degree of accuracy is required (i.e. <10%). This is because such a circuit would require an analogue multiplier to derive a power term; such circuits suffer from poor calibration and relatively large output offsets. Commercially available multipliers which offer increased accuracy are individually trimmed by the manufacturer and are thus many orders of magnitude more expensive than their non-trimmed counterparts. If the SSPC were to utilise such components this would have an adverse affect on its economic viability.

In addition to the topic of model accuracy, another important consideration is that of the time taken for the model to produce a temperature prediction output. A fast response time allows a far tighter tolerance to be placed on the die temperature at which the SSPC should turn off. This is because it will have detected the event that caused the die heating from the very first instant. Similarly a fast response time will accommodate the small temperature changes caused by the possibility of short (<50μs) power transients. Although these would not raise the die temperature very much, if they are ignored they may affect the overall accuracy of the protection mechanism. The analogue solution by its very nature will incur the minimum of delay. The voltage change across the first capacitor, representing die temperature, will mirror in time almost exactly what is happening with the die temperature in reality. The only limitation to this is in the analogue circuit response time which converts a measure of the power dissipated in the die to the current directed into the RC chain. For most practical circuits however, this will at worst represent only a few microseconds. The numerical model by contrast will be constrained on a number of counts, namely: the complexity of the model, i.e. number

of nodal elements, the processor execution time and the speed of digitising voltage and current values. From a commercial perspective, if the SSPC is to be economically viable the processing element cannot be too specialised since such devices normally incur a price premium. In addition, the upper limit on iteration time is constrained by Equation 8.19. If this criterion is not met, numerical instability will quickly ensue and any model prediction will be meaningless. Although these constraints introduce significant difficulties to a numerical implementation it will be shown later in both this chapter and in Chapter 9 that by the addition of very simple hardware and by placing a limit on the maximum dissipation in a MOSFET die these constraints may be effectively minimised.

A final consideration for any practical SSPC prediction model is that the solution should be flexible enough to easily accommodate different semiconductor die sizes or a differing number of dies. Section 3.4.2 provided a breakdown of current ratings required for the protection devices in a typical aircraft. The most economic method of matching the spread of current demands is to vary the silicon content of the switching element accordingly. With the analogue solution this will require that a new model be constructed for every change. Such a task will incur all the implementation problems previously discussed. The numerical solution is somewhat easier in that a differing number of dies can be accommodated by applying a simple scaling factor to the calculation which will divide the power by the number of devices present. Similarly if a different semiconductor is used which has a different die geometry such a change will only require a small adjustment to the software parameter values which define the model. Such a task is easy to perform and requires no hardware changes to the control configuration.

From the above discussion it is evident that each method has its merits and disadvantages. Despite the fact no references can be found of any prior use of the numerical method as a silicon protection technique, on balance the solution is considered to be the most appropriate and consequently will be developed further.

8.5 Derivation of a Run Time MOSFET Model

In this section an explanation is provided of the steps taken to develop a numerical model which is sufficiently condensed to be executed in real time. As briefly discussed in the previous section, the major constraint is the computational efficiency of the algorithm. In order to achieve numerical stability, the time to execute (sampling time) must be shorter than the smallest nodal time constant in the model. The most basic model which mirrors reality is to represent the structure in one dimension only as shown in Figure 8.5.

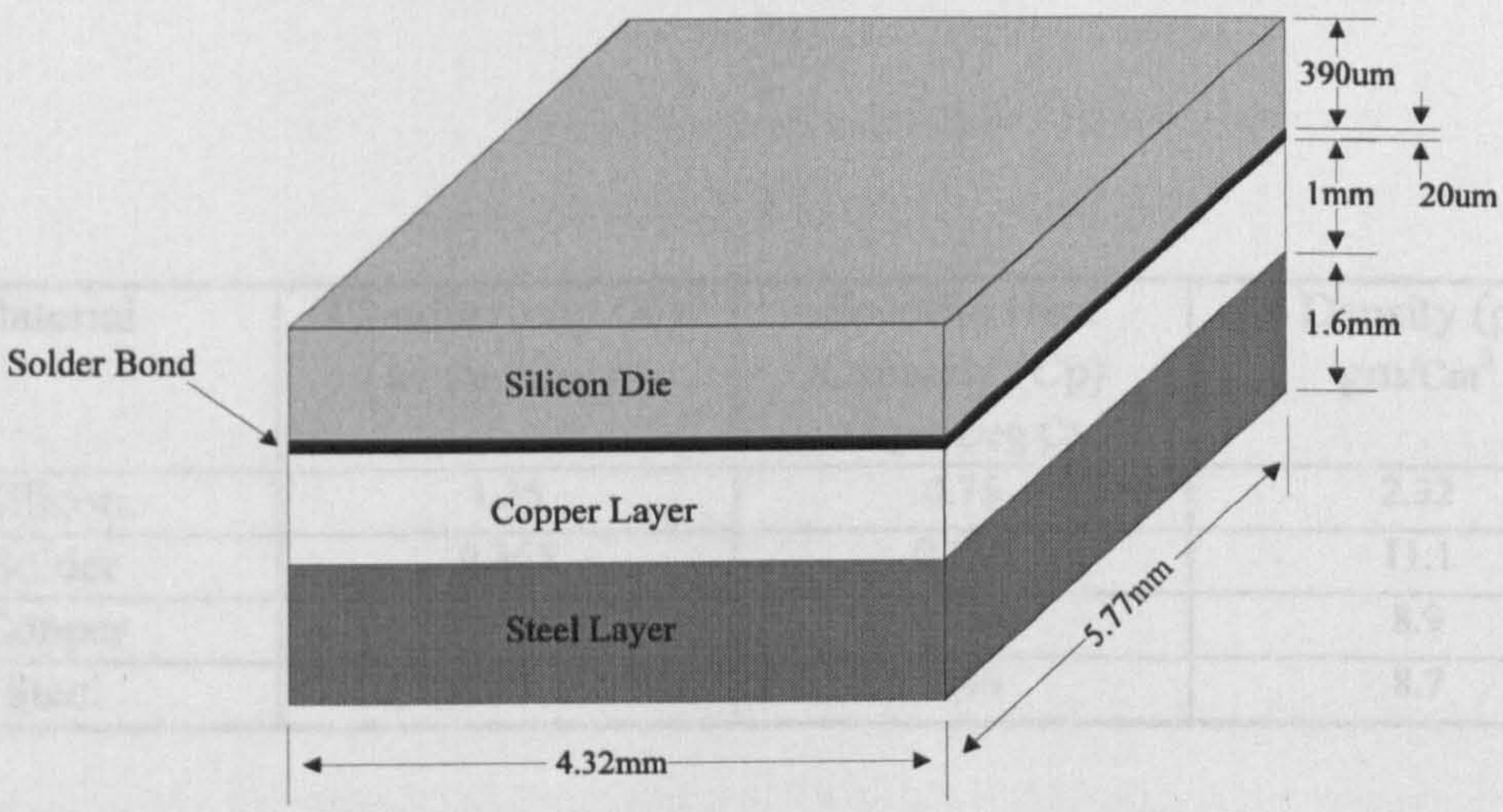


Figure 8.5 One Dimensional MOSFET Die and Package Model

In the model each of the MOSFET structural elements are represented, namely, the die, solder bond, copper layer and for the IRF044 test device the steel layer. The assumption is made that heat is generated in a plane which has the same area as the entire top surface of the die. Similarly the model also assumes that the temperature of each layer will change uniformly as a function of time. The reference temperature interfaces with the model on the lower surface of the steel layer. For modelling purposes this temperature is static; in the real SSPC implementation however this temperature will be a measured quantity.

A simulation program which utilised Equation 8.17 was written in C++ and compiled to run on a PC platform. This program uses as its input parameters the value of power dissipated in the die (in watts), the time step (in seconds) and the value of R_{th} and C_{th} for each of the modelled layers. From this information the program can iteratively calculate the temperature of each layer as a function of time.

Figure 8.6 presents the output of this program model for an IRF044 with a simulated die power dissipation of 500W, also displayed is the IR measured temperature for the corresponding power. The value of R_{th} and C_{th} were calculated from the physical values given in Table 8.1 (note the material properties are quoted at the 50 Degrees C value [45]).

Material	Conductivity (K) (W/ Cm^3/Deg C)	Specific Heat Capacity (Cp) (J/gm/Deg C)	Density (ρ) gm/Cm^3
Silicon	1.35	0.75	2.32
Solder	0.365	0.135	11.1
Copper	3.96	0.388	8.9
Steel	0.5	0.46	8.7

Table 8.1 Physical Layer Values for MOSFET Structure

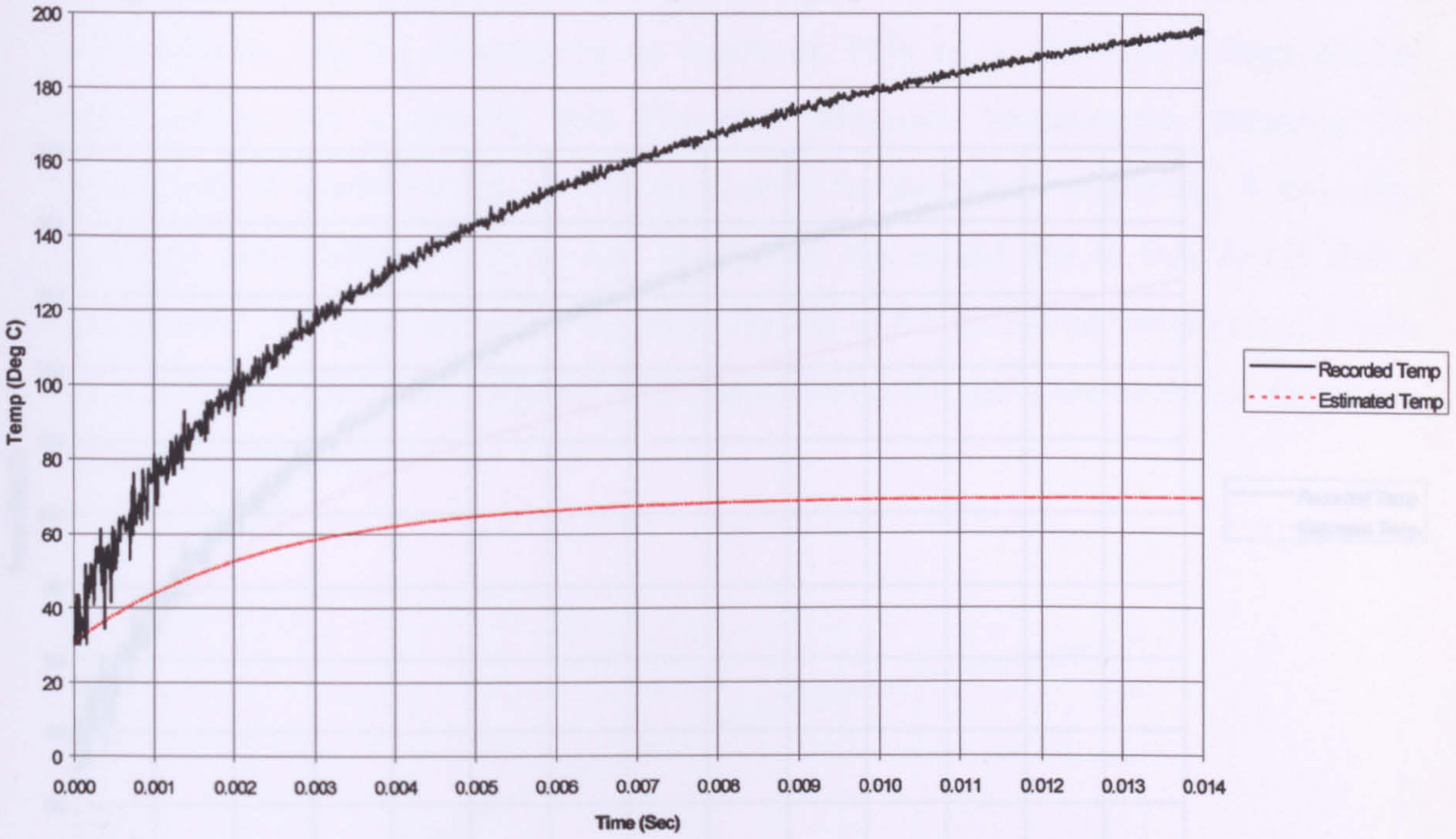


Figure 8.6 IRF044 Comparison of 4 Layer Model and Recorded Temperature for a Die Power Dissipation of 500W

From Figure 8.6 it is evident that the output of the 4 layer model described deviates significantly from the measured temperature. This large deviation is a result of the die being modelled as a single lumped parameter. The relatively large thermal time constant of the total modelled die in relation to the much smaller thermal time constant of the real die heat dissipating area means that the modelled temperature rises far more slowly over the time of interest than will occur in reality. Similarly another reason for the large deviation is the fact that a single node representing the die in such a model will result in only half the die thermal resistance being considered as part of the calculation. The real heat dissipating region is a thin layer at the top of the die and consequently the thermal resistance will be much larger than the value used in this simple model. The effect of this discrepancy is to reduce the overall predicted temperature even further. After several modelling iterations it was found that a good compromise could be obtained by modelling the die as two layers with the top layer having 33.3% of the total die volume

and the bottom layer having the remainder. Figure 8.7 details the output of this configuration for the same modelled die power dissipation.

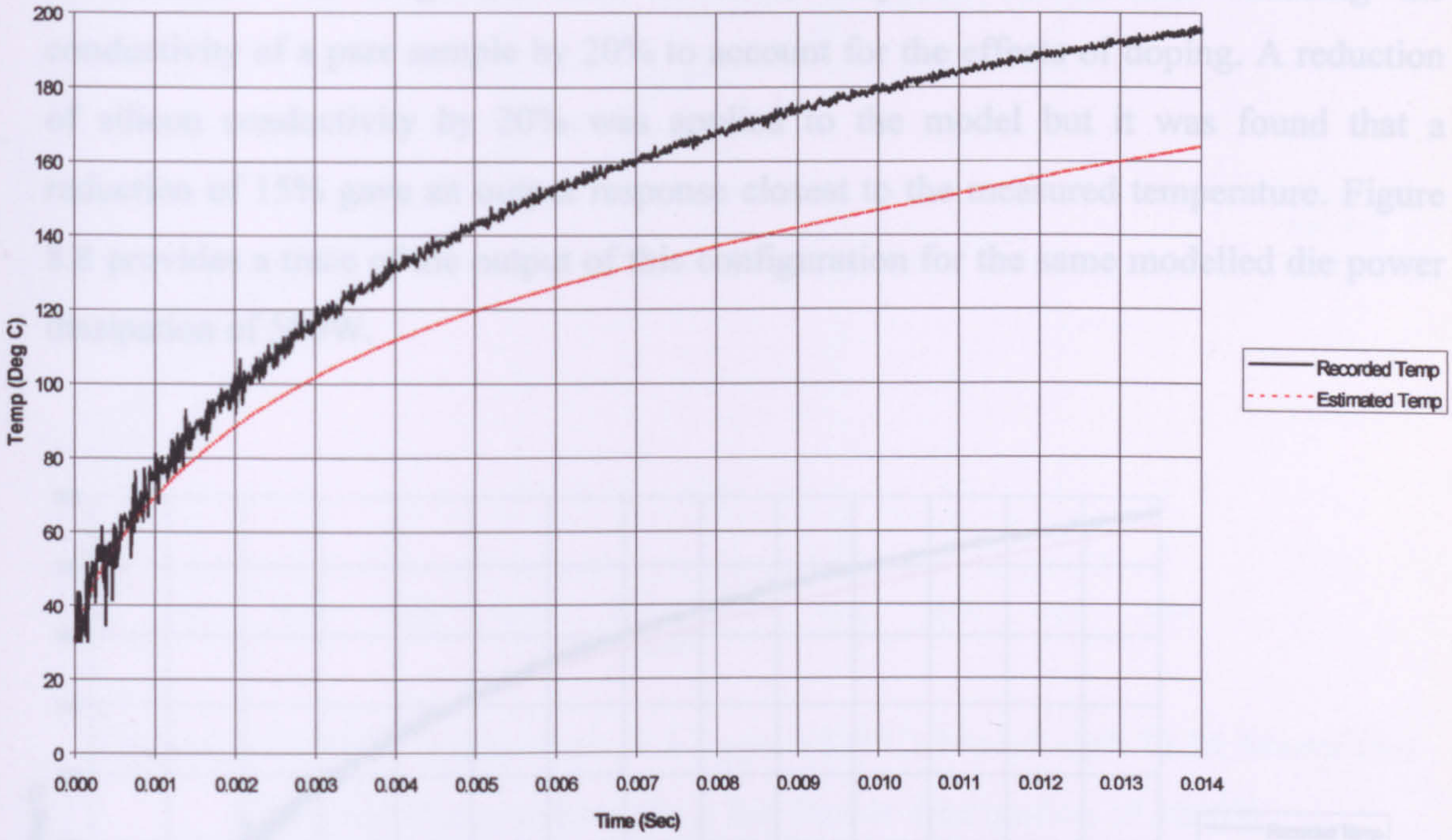


Figure 8.7 IRF044 Comparison of 5 Layer Model and Recorded Temperature for a Die Power Dissipation of 500W

From Figure 8.7 it is again evident that the model deviates significantly from the measured temperature profile. This deviation was found to be caused by two factors associated with the value of silicon conductivity used in the model.

The first factor has previously been discussed in Section 8.4, that is, the value of silicon conductivity changes markedly with temperature. In consideration of this, the model was modified to include Equation 8.20 for the calculation of the silicon R_{th}, for both top and bottom die layers. This modification means that the most recent iteratively calculated silicon layer temperature is used in the calculation of R_{th} for the same layer in the next iteration.

The second factor associated with silicon conductivity relates to the change in conductivity caused by doping. Maycock [83] reports that the thermal conductivity of a semiconductor can be lowered by as much as 30% as a result of a high doping concentration. As a general rule however, Maycock recommends reducing the conductivity of a pure sample by 20% to account for the effects of doping. A reduction of silicon conductivity by 20% was applied to the model but it was found that a reduction of 15% gave an output response closest to the measured temperature. Figure 8.8 provides a trace of the output of this configuration for the same modelled die power dissipation of 500W.

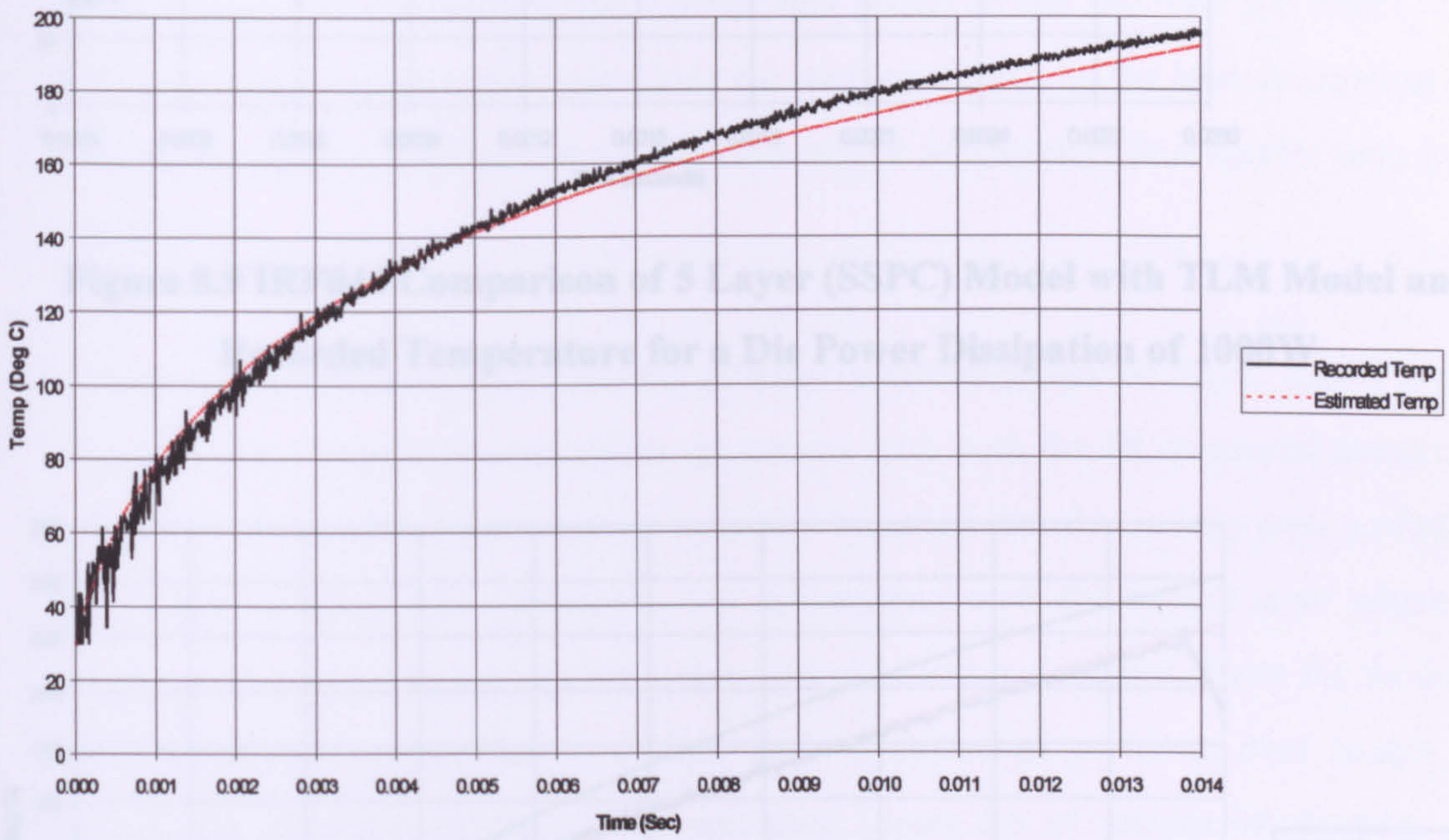


Figure 8.8 IRF044 Comparison of 5 Layer Model with Silicon Conductivity Compensation Die Power Dissipation of 500W

From Figure 8.8 it can be observed that the 5 layer model containing the silicon conductivity compensation terms generates an output which is very close to that of the measured temperature value. Figures 8.9 and 8.10 display the output for this model at die power dissipation of 1000W and 2000W respectively. In addition to the model output the graphs also display an overlay of the IR recorded die temperature and the TLM simulator output for the same dissipated power.

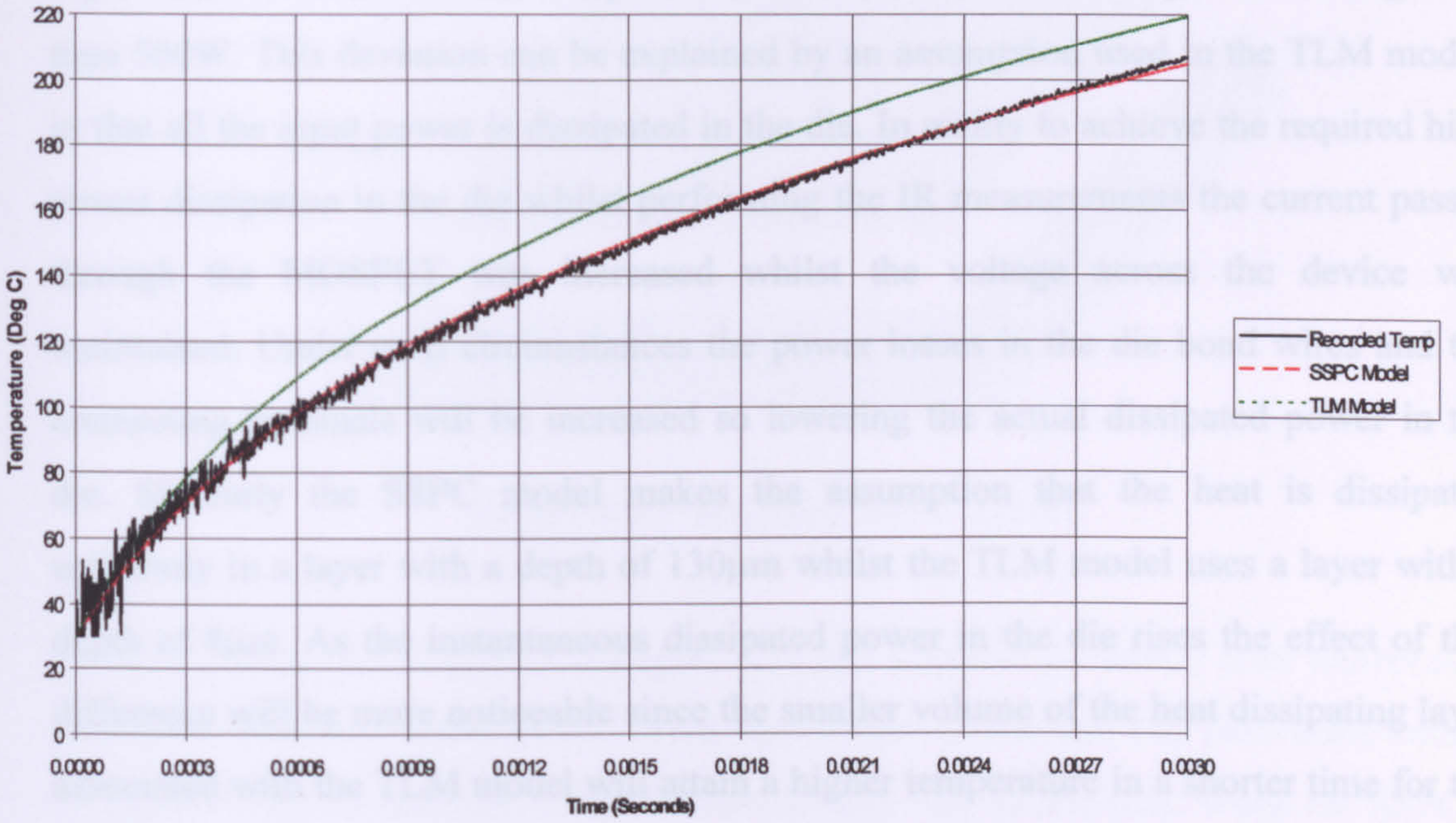


Figure 8.9 IRF044 Comparison of 5 Layer (SSPC) Model with TLM Model and Recorded Temperature for a Die Power Dissipation of 1000W

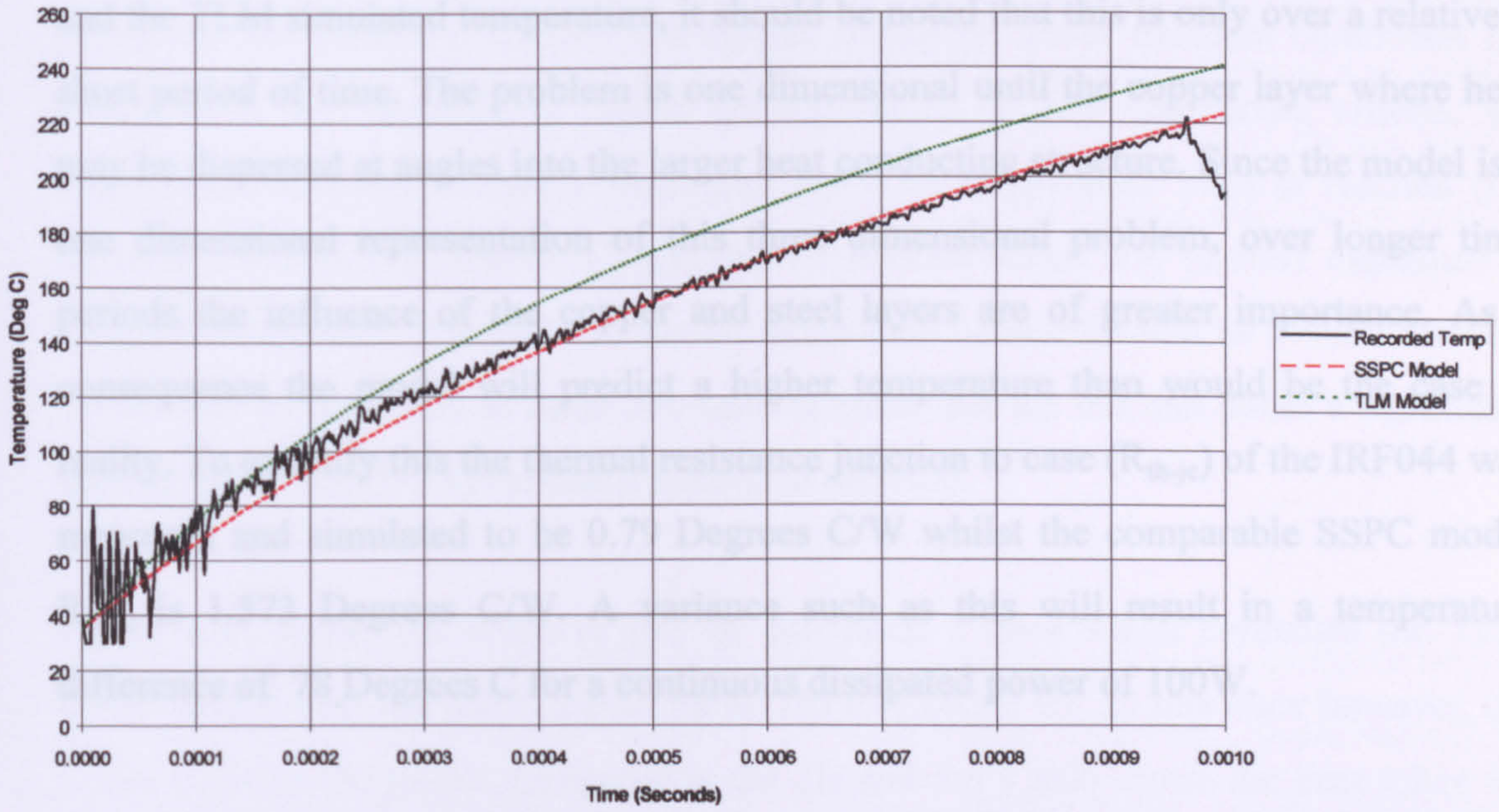


Figure 8.10 IRF044 Comparison of 5 Layer (SSPC) Model with TLM Model and Recorded Temperature for a Die Power Dissipation of 2000W

It is evident from these diagrams that the TLM model predicts a temperature slightly higher than both the recorded temperature and the SSPC model for power levels greater than 500W. This deviation can be explained by an assumption used in the TLM model, in that all the input power is dissipated in the die. In reality to achieve the required high power dissipation in the die whilst performing the IR measurements the current passed through the MOSFET was increased whilst the voltage across the device was maintained. Under such circumstances the power losses in the die bond wires and the connecting terminals will be increased so lowering the actual dissipated power in the die. Similarly the SSPC model makes the assumption that the heat is dissipated uniformly in a layer with a depth of 130μm whilst the TLM model uses a layer with a depth of 8μm. As the instantaneous dissipated power in the die rises the effect of this difference will be more noticeable since the smaller volume of the heat dissipating layer associated with the TLM model will attain a higher temperature in a shorter time for the same power.

A final consideration in the modelling process is that although the SSPC model predicts a temperature which is in reasonable agreement with both the IR measured temperature and the TLM simulated temperature, it should be noted that this is only over a relatively short period of time. The problem is one dimensional until the copper layer where heat may be dispersed at angles into the larger heat conducting structure. Since the model is a one dimensional representation of this three dimensional problem, over longer time periods the influence of the copper and steel layers are of greater importance. As a consequence the model will predict a higher temperature than would be the case in reality. To quantify this the thermal resistance junction to case ($R_{th\text{-}jc}$) of the IRF044 was measured and simulated to be 0.79 Degrees C/W whilst the comparable SSPC model $R_{th\text{-}jc}$ is 1.573 Degrees C/W. A variance such as this will result in a temperature difference of 78 Degrees C for a continuous dissipated power of 100W.

One method of reducing this difference is to model both the copper and steel layers in a pseudo three dimensional form [45] [82] as shown in Figure 8.11.

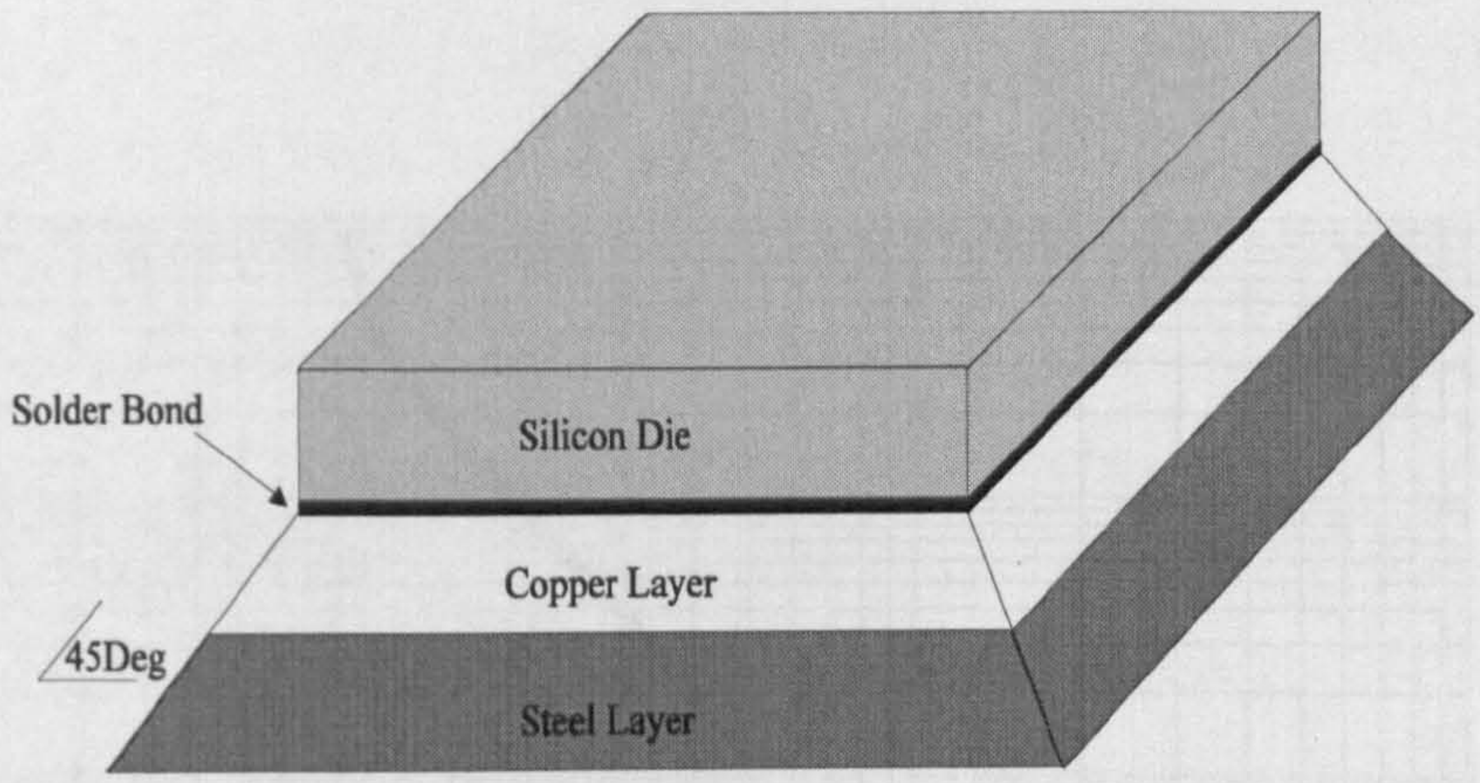


Figure 8.11 Modified SSPC Model

Although the model displayed in Figure 8.10 will improve the steady state temperature prediction accuracy, under normal SSPC operational conditions, any inaccuracy caused by representing the problem in one dimension only will be minimal. When the SSPC is fully conducting, the power dissipated in each MOSFET die will be under 3W (this will be examined in Chapter 9) and the temperature difference will be in the order of 2.2 Degrees C. It will be shown in the following chapter that a temperature difference as small as this falls well within the bounds of an acceptable tolerance band which must be placed on any predicted temperature output. Similarly, under transient conditions the effects of a one dimensional model are minimised by two operational criteria: the requirement that the MOSFET must turn off if its temperature limit is reached (i.e. between 150 and 175 Degrees C) and that for reasons which will be fully explained in Chapter 9 the power dissipated in the die under fault conditions will be several hundred Watts. The combination of these two criteria mean that the die will avoid a significant heating phase which is more than 1 second in duration.

Figure 8.12 shows the effect of this by providing a trace which compares the TLM model output with the SSPC model for an IRF044 MOSFET. In this trace however, the x axis displays the power dissipated in the die and the y axis shows the time taken for the hottest part of the die to reach 175 Degrees C (Note the ambient temperature was fixed at 25 Degrees C).

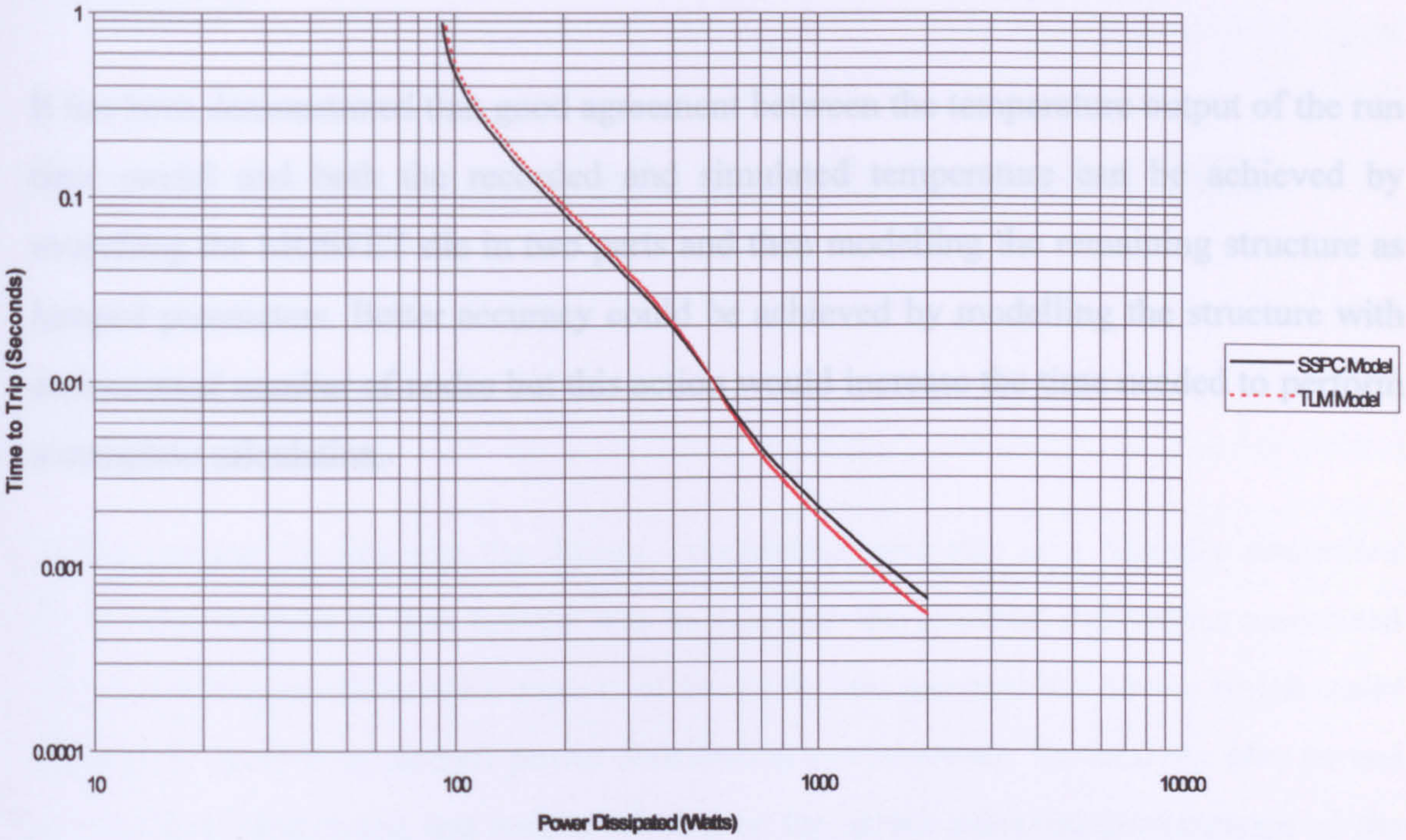


Figure 8.12 Power Dissipated versus Time to Reach 175 Degrees C for IRF044

From a comparison of the two response curves presented in Figure 8.12 it is evident that the SSPC model shows reasonable agreement with the TLM output over the one second period of interest. As the power dissipation approaches 1000W however the noticeable deviation caused by the volume of the heat dissipating area as discussed earlier can be observed.

8.6 Conclusions

This chapter has provided an assessment of the temperature prediction methods which could be applied to estimate the MOSFET die temperature in an SSPC implementation. Of the available techniques, the analogue method and the digital (finite difference) method was considered to be the most suitable for this application. Of these, the digital technique was favoured owing to the ease in which it can be configured for different

MOSFET solutions and its ability to accommodate physical phenomena which occurs as a result of temperature change.

It has been demonstrated that good agreement between the temperature output of the run time model and both the recorded and simulated temperature can be achieved by modelling the MOSFET die in two parts and then modelling the remaining structure as lumped parameters. Better accuracy could be achieved by modelling the structure with an increased number of nodes but this action would increase the time needed to perform a complete calculation.

Chapter 9

Practical Implementation of a Digitally Controlled SSPC

9.1 Introduction

In this chapter we describe the design, construction and test of a digitally controlled SSPC. The purpose of this activity was to examine the practical difficulties associated with translating the theoretical aspects of the study into a protection device which could feasibly be used in an aircraft power distribution environment. The activity also served as a method of deriving test results relating to the actual achieved performance of the SSPC implementation compared to that of the theoretical response.

The chapter is structured into three parts: The first part details the important design decisions and the rationale relating to key attributes of the design. The second part describes the general functionality and operational characteristics of the SSPC device. The final section details the tests performed on the SSPC and presents the results of these tests.

9.2 Voltage and Current Rating of the Test Device

The first issue of the SSPC development was to determine the voltage and current levels to which the device would be subject. Chapter 3 provided details of the aircraft voltage supplies which are presently used, together with a breakdown of typical aircraft electrical load currents. Similarly, Chapter 2 provided a rationale for why direct current voltage supplies are increasingly favoured by both the airframe manufacturers and the

suppliers of electronic equipment. In view of this emphasis on dc power systems, it was decided that two SSPC's would be constructed. One was to operate at 28V dc and the other at 270V dc. It was considered that this focus on dc systems would not be too great a penalty since an ac SSPC could be derived relatively easily by placing a dc SSPC within a simple bridge rectifier configuration.

As will be discussed later, the maximum current handling capability of the SSPC was constrained by the capability of the test equipment to provide enough load current for meaningful experimentation. In view of this, the target steady state maximum current capability of the 28V device was set at 60 Amps with an inrush capability of 240A. Similarly, the maximum steady state current for the 270V part was set at 10A with an inrush capability of 40A. This inrush capability was determined from the results of a proprietary load analysis on a state of the art aircraft utilising dc supplies [84].

Although these values represent design targets, one of the aims of the study was to establish the ease in which load current requirements could be met by adjusting the number of switching devices in the SSPC. As a consequence, the design philosophy of the SSPC was that a universal control element could be applied to a variable number of switching devices (up to a physical maximum) whereby no additional hardware modifications would be necessary.

9.3 MOSFET Selection

One of the design criteria for a practical SSPC is that the on state voltage drop across the device should be as small as possible. As was previously discussed in Chapter 3, one of the ways to reduce conduction drop is to match the MOSFET voltage rating as closely as possible to the voltage requirement of the SSPC. In addition, as the MOSFET die size is increased the saturated on resistance is also normally reduced. For commercially available devices the device cost increases significantly once die proportions go beyond size 5 (i.e. 6.53 × 6.53 mm). Consequently this makes size 5 the

most attractive from a commercial viewpoint. From a performance standpoint, the die temperature measurement and simulation activities detailed in Chapter 7 produced a significant quantity of thermal information relating to a TO3 packaged device. Despite this, the TO3 was only selected because it allowed easy access to the die for the purposes of taking IR measurements. In reality this is a very poor package compared to its modern counterparts such as the TO3P or the TO247. The reason for this poor performance is that the steel package of the TO3 is a relatively inefficient conductor of heat with the result that the $R_{th\text{-}jc}$ is approximately 20% higher than that of a similar TO247 packaged device. The steel package is also a disadvantage electrically, in that it increases the inductance of the gate and source pins.

In consideration these points the IRFP054 [35] was selected for the 28V SSPC and the IRFP450 [35] was selected for the 270V part. The IRFP054 MOSFET is a 60V device with an Rds_{on} of 14mΩ @25 Degrees C and a maximum continuous drain current value 70A (Note this value assumes the base is maintained at a constant 25 Degrees C). The IRFP450 MOSFET is rated at 500V, has an Rds_{on} of 400mΩ @25 Degrees C and a maximum continuous drain current value 14A (again this value assumes the base is maintained at a constant 25 Degrees C). Both these devices use a TO247 package which does not have a steel layer, thus simplifying the thermal model and reducing execution time.

9.3.1 T0247 Thermal Analysis

In order to construct and to verify an SSPC executable thermal model for a T0247 package, it was again necessary to perform some of the tasks previously detailed in Chapter 7. It was not possible to make infrared die temperature measurements on the device owing to the fact the MOSFET die is totally encased in plastic resin. Any attempt to expose the die normally results in its destruction. As an alternative, verification was focused on again creating a detailed TLM thermal model which could be used to assess

the accuracy of the SSPC run time model. The fact that no measured results existed was not seen as a major issue given the previous good agreement between the infrared thermal measurements and the TO3 TLM model output. In order to create a TO247 TLM model however, it was necessary to section some devices in the manner previously described in Section 7.7.1. A total of 12 devices (six IRFP054 and six IRFP450) derived from two differing batch numbers were sectioned and the items of interest measured (i.e. die thickness, solder thickness etc.). The findings were similar to that experienced with the T03 packaged device, in that the items of interest were very tightly controlled by the device manufacturer, consequently any variation was too small to be of any significance. Figure 9.1 shows a photograph of one of the sectioned TO247 MOSFET devices.

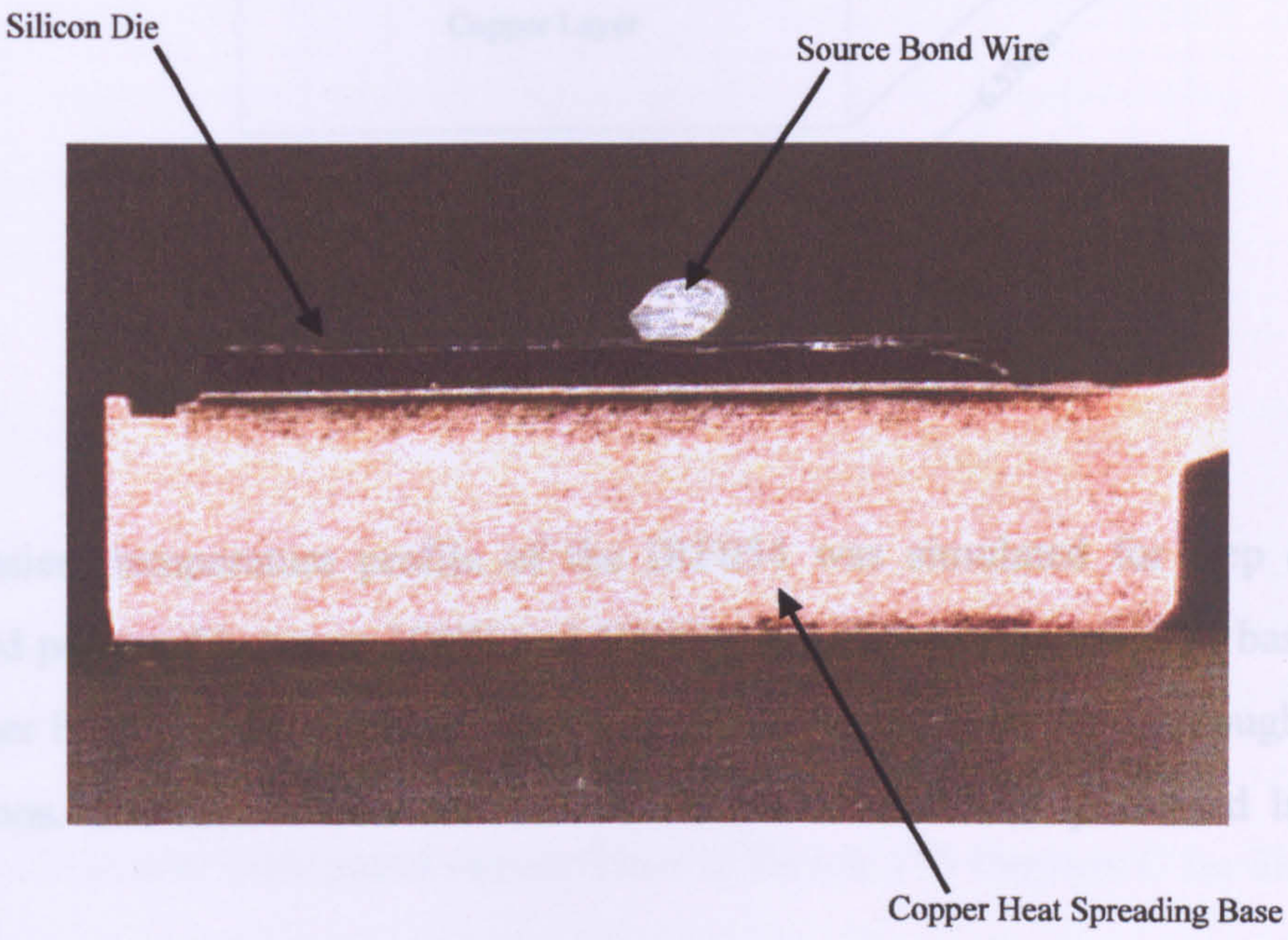


Figure 9.1 Photograph of Sectioned TO247

From Figure 9.1 it can be observed that the copper heat spreading base is far smaller in relation to the silicon die area than in the previous TO3 example. Although the copper base extends further in the direction of the terminal pins, it is evident from the photograph that providing the base is attached to a good thermal sink, the heat flow problem is in reality more one dimensional than with the T03 device.

In consideration of this fact Figure 9.2 presents the final thermal model of an IRF054 used for the transient TLM simulation. For this model the layer dimensions were again derived from the physical examination of the device.

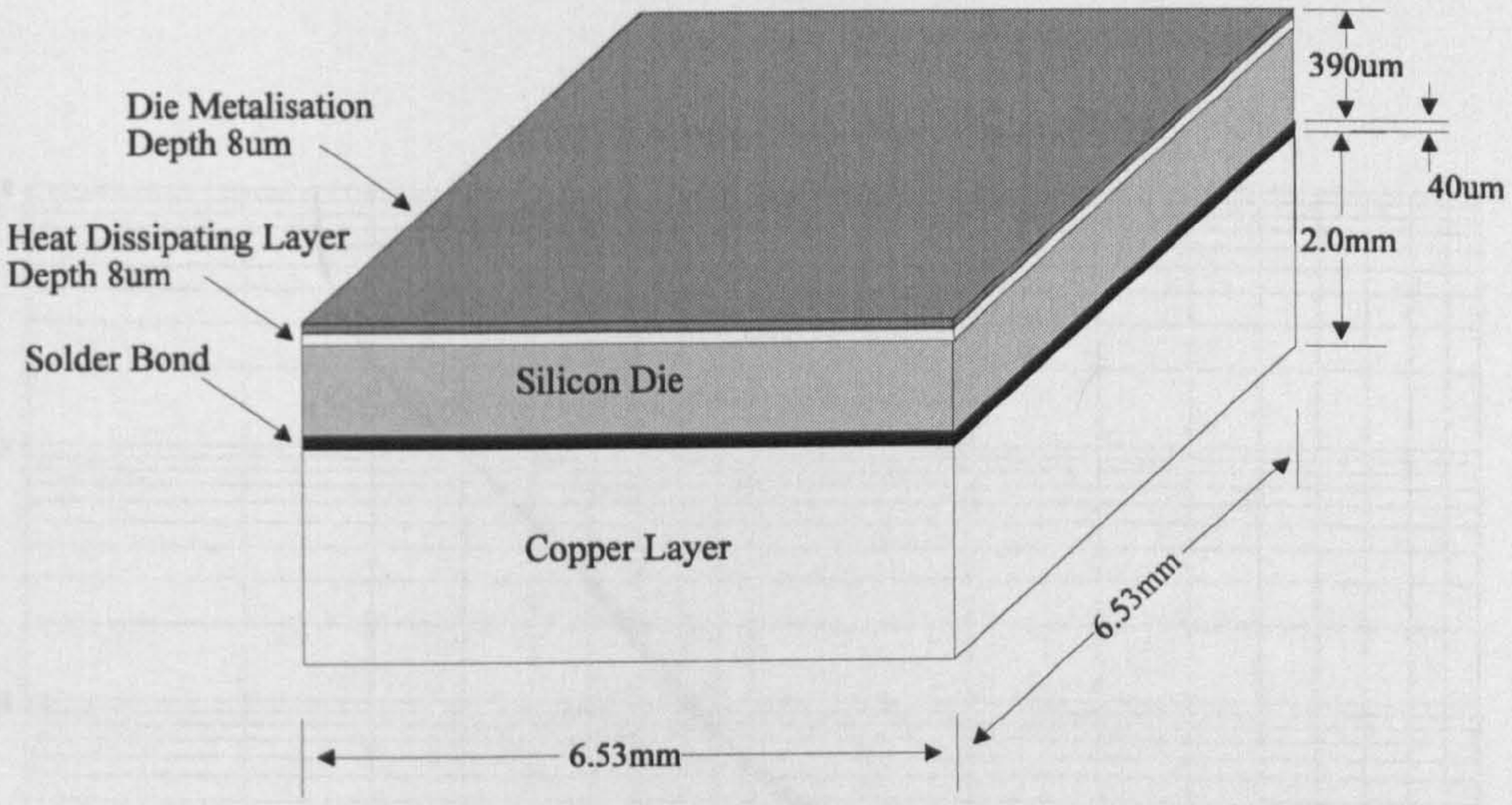


Figure 9.2 TLM Model of the IRFP054

The transient temperature profile of the IRF054 was simulated for step changes in dissipated power of between 100W and 4000W in 100W increments. The base to which the copper layer interfaces was modelled at a constant 25 Degrees C throughout all the simulations. The results from the TO247 TLM model will be presented later in this chapter.

9.3.2 SSPC Die Temperature Prediction Model Generation

The approach to generating a run time thermal model for the MOSFET's used in the SSPC was to reproduce exactly the modelling techniques derived in section 8.4. The die was once more modelled in two halves, with the top portion occupying a third of the total die volume and the bottom portion occupying the remaining two thirds. Both layers were modelled with the silicon conductivity value varying as a function of temperature.

The remaining solder and copper layers were each modelled as lumped parameters. Figure 9.3 presents the SSPC run time model output compared with the TLM simulator response, the x axis displays the power dissipated in the die and the y axis shows the time taken for the hottest part of the die to reach 175 Degrees C (Note the ambient temperature was fixed at 25 Degrees C).

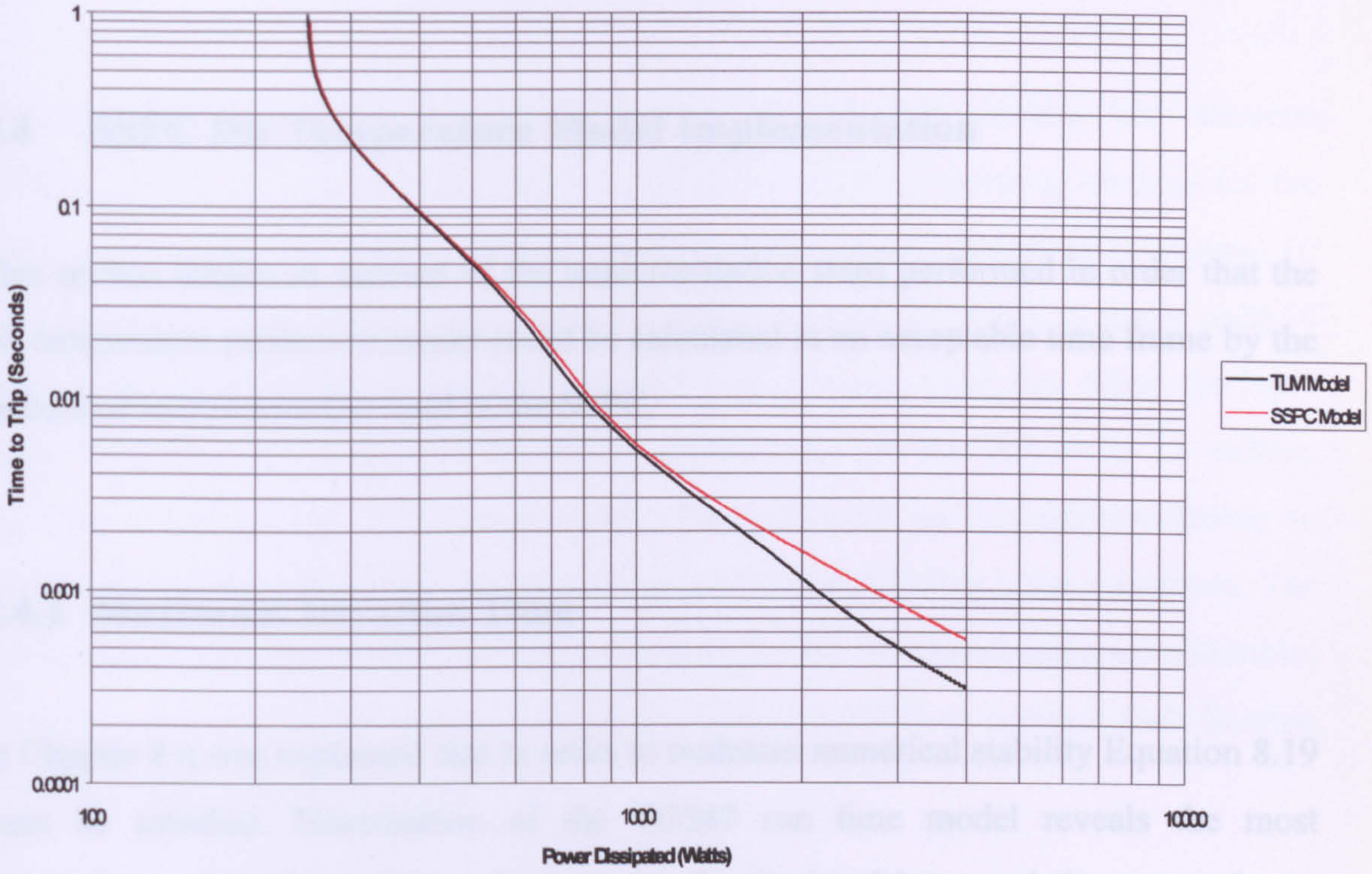


Figure 9.3 Power Dissipated versus Time to Reach 175 Degrees C for IRFP054

From a comparison of the two curves it is evident that the SSPC model shows reasonably good agreement with the TLM output over the one second period of interest. As the power dissipation approaches 1500W however, deviation of the two response curves can again be observed; the cause of this deviation is due to the same model differences outlined in Section 8.4 (i.e. the volume of the heat dissipating area). It should be noted that the TLM model parameters relate to an IRFP054 which is a 60V device, and as such, the heat dissipating area has a vertical depth which is in the region of 8μm (see figure 9.2). The IRFP450 being a higher voltage device will have a thicker

epitaxial layer which means a corresponding larger heat dissipating area. As was highlighted in Section 7.3, this thickness can be as much as 100μm. Despite this increase, it is still smaller than the one third of die thickness used in the run time model. The outcome of this is that the model is still valid for the higher voltage device and should be slightly more accurate at high levels of dissipated power owing to the convergence in size of the physical and modelled heat dissipating regions.

9.4 SSPC Die Temperature Model Implementation

This section details an account of the implementation steps performed in order that the die temperature prediction model could be calculated in an acceptable time frame by the embedded microcontroller used in the SSPC.

9.4.1 Maximum Iteration Time

In Chapter 8 it was explained that in order to maintain numerical stability Equation 8.19 must be satisfied. Examination of the TO247 run time model reveals the most demanding nodal relationship to be between the die bond layer and the copper layer. Using Equation 8.19 the maximum iteration time (Δt) for the model is determined as 1.815×10^{-4} seconds (where C_{th} bond = 0.0025 J/Degrees C, R_{th} Bond = 0.0268 Degrees C/W and R_{th} copper = 0.1184 Degrees C/W). This time represents the absolute maximum execution time allowable (in reality, a shorter time is required since the processor will also be performing the I^2t protection and the general control functions i.e. responding to on/off requests, checking status etc.).

As was previously discussed in Section 8.4, from a performance standpoint the iteration time should be as small as possible as this will reduce any tolerance that needs to be applied to the trip point (the magnitude of this tolerance will be examined later in the

chapter). From a commercial perspective however, if the SSPC is to be a viable alternative to an electro-mechanical solution it cannot rely on any expensive or specialised computing device. In considering the conflicting requirements a compromise target iteration cycle time was initially set at 100μs or less.

9.4.2 Microcontroller Selection and Performance Evaluation

Following an evaluation of contemporary microprocessing devices the Siemens SAB167CR Microcontroller [85] was selected as the digital processing element for the SSPC implementation. This device has a 16 bit architecture and features a 16 channel 10 bit analogue to digital converter (9.8μs minimum conversion time), 5 timer units, 4 pulse width modulator channels and 2 serial communication modules. When the input clock frequency is 20Mhz the maximum performance of the device is 10 million instructions per second. Benchmark tests were performed on this microcontroller to assess the execution time for a number of single precision floating point operations. The bench mark tests were written in ANSI C but made use of custom supplied assembler routines to perform the arithmetic operations. The time taken to perform each floating point operation was found to be:

Multiplication of two variables = 6.6μs

Division of two variables = 6.8μs

Addition of two variables = 13.6μs

Subtraction of two variables = 7.4μs

The run time numerical model described in Section 9.3.2 requires the following floating point operations: 6 multiplications, 12 divisions, 8 subtractions and 7 additions. This equates to a total calculation time of 275.6μS. In reality the actual calculation time was slightly longer than this owing to other instructions required to move data in and out of working registers and compare the peak temperature with the trip level. It is apparent that even when the microcontroller is operating at full speed the calculation time for a

single iteration of the die temperature prediction program is significantly longer than the maximum allowable time step. One solution might be to use a more powerful computing device capable of performing the calculation within the required time. However, as has already been stated, such an approach would have a severe impact on the economic viability of the final SSPC solution. The other approach involves integerising the majority of the calculation and making use of look-up tables to provide the required floating point precision. The philosophy of this solution is centred on the fact that integer (fixed point) calculations are relatively fast to perform on modern microprocessors (SAB167CR typical execution time was 100ns); similarly the access to a look up table entry is typically performed in 2 instruction cycles (200ns). Such a scheme provided an eventual solution to the real time die temperature prediction calculation problem. The following section provides a description of the method developed for program integerisation.

9.4.3 Integerisation of Die Temperature Calculation

For the purposes of clarity the previous equation 8.19 can be rearranged to that of equation 9.1.

$$T_i^{p+1} = T_i^p + \frac{\Delta t}{C_i}\left[q_i - \sum_j \frac{T_i^p - T_j^p}{R_{ij}}\right] \quad \text{-(9.1)}$$

Assuming the time step Δt is constant and so too are the physical properties R_{th} and C_{th}, the operations involving these quantities can be mechanised in the format of a lookup table where the constituent parts are given by :

$$a = \left[\sum_j \frac{c}{R_{ij}}\right] \quad \text{-(9.2)} \qquad b = \frac{\Delta t}{C_i}[d] \quad \text{-(9.3)}$$

Equations 9.2 and 9.3 represent the two lookup table contents required for the solution of Equation 9.1. The variables ***c*** and ***d*** represent the integer index into the table and the variables ***a*** and ***b*** represent the table contents. In order for this scheme to work however, it is necessary to define a number of operational characteristics relating to the numerical implementation.

The first unknown is the maximum value which will reside in the table contents. To resolve this, it is first necessary to know the maximum input power for each stage in the equation. For the SSPC implementation this maximum input power is simply the maximum simultaneous voltage and current to which the modelled die will be subject. Once having established the input power it is then possible to determine the maximum differential steady state temperature between the node of interest and the next adjoining node (i.e. the next node in the direction of heat flow). This quantity is found by the product of maximum input power and the path resistance between the adjoining nodes of interest (R_{ij}). The content of each lookup variable for Equation 9.2 may then be determined using the following term:

$$Contents\_a_l = \left(\frac{T}{n} \times \frac{1}{\frac{\sum R_{ij}}{P} \times 2^y} \right) \times l \qquad \text{- (9.4)}$$

where $Contents\_a_l$ is the table value, T is the maximum temperature differential between the nodes (note this value must be to the nearest rounded up integer power of 2, i.e. a binary sequence number), n is the maximum size of the look-up table, R_{ij} is the path thermal resistance between the adjoining nodes, P is the maximum input power (note this value must again be to the nearest rounded up integer power of 2), y is the number of bits the content value is represented in and l is the table index. Similarly the maximum value in the table representing Equation 9.3 will be the product of the maximum power input and $\Delta t/C_i$. This value represents the largest temperature

increment (ΔT_{max}) for that node over the time step Δt. Thus the table contents can be formulated using the following expression:

$$Contents\_b_l = \left(\frac{\frac{P}{n} \times \frac{\Delta t}{C_l} \times 2^y}{\Delta T_{max}} \right) \times l \qquad -(9.5)$$

where $Contents\_b_l$ is the table value, P is the maximum input power (note this value must be to the nearest rounded up integer power of 2), n is the maximum size of the look-up table, C_l is the thermal capacitance of the node, y is the number of bits the content value is represented in and l is the table index.

In order to perform the remainder of the calculation it was necessary to determine the position of the decimal point in the integer representation of the temperature value. For the die temperature problem it was considered that the calculated temperature would not exceed the rated temperature limit for the die. This temperature for the IRFP054 is 175 Degrees C, and consequently this value may be represented as an 8 bit mantissa giving a maximum calculable temperature of 255 Degrees C. The remainder of the word represents the fractional fixed point exponent. When adding and subtracting such values it was important to ensure the two numbers shared the same fixed decimal point position. Where this was not the case (as in most of the look-up table contents) it was necessary to shift the bit positions up or down in one of the values until the decimal point positions were aligned. The drawback of this approach is if the binary word size is not sufficiently large significant precision can be lost owing to the fact bits in the exponent are usually discarded.

For the SSPC implementation the size of each table lookup was standardised at 8192 locations, this represented a compromise between the estimated resolution requirement and the total quantity of memory available for the SSPC implementation (this was fixed at 128K bytes). One problem associated with the look-up table approach however, was

that a large number of look-up tables were required to implement the variation of silicon conductivity with temperature. The problem centred on the fact Equation 9.2 would have two input variables (i.e. c and R_{ij}) and this presented a large number of possible combinations.

One solution to the problem is to provide sufficient memory to accommodate the increased number of table look-ups. Such an approach would however increase the cost and size of the SSPC implementation. Another investigated solution involved performing part of the equation using floating point arithmetic and then casting the result into an integer format in order to perform the remainder using the look-up table approach. Although this solution proved relatively successful, even after optimisation (i.e. coding in assembler) the execution time could not be reduced beyond 114μs. It would have been possible to use a time step of about 150μs to accommodate the other SSPC operations, but as has already been discussed such a time step would require a larger tolerance to be applied to the trip point. In investigating this problem it was discovered that a good temperature prediction response over the time of interest could be obtained by modelling the top 33% of the die with a silicon conductivity at a 140 Degrees C value and the remaining part with a conductivity at a 150 Degrees C value. Despite the fact with this solution will introduce a steady state error, for reasons that have previously been discussed in Section 8.4 this error is less than 0.4 Degrees C when the device is fully conducting.

Figure 9.4 presents a comparison of this model with the TLM model output and the varying conductivity model.

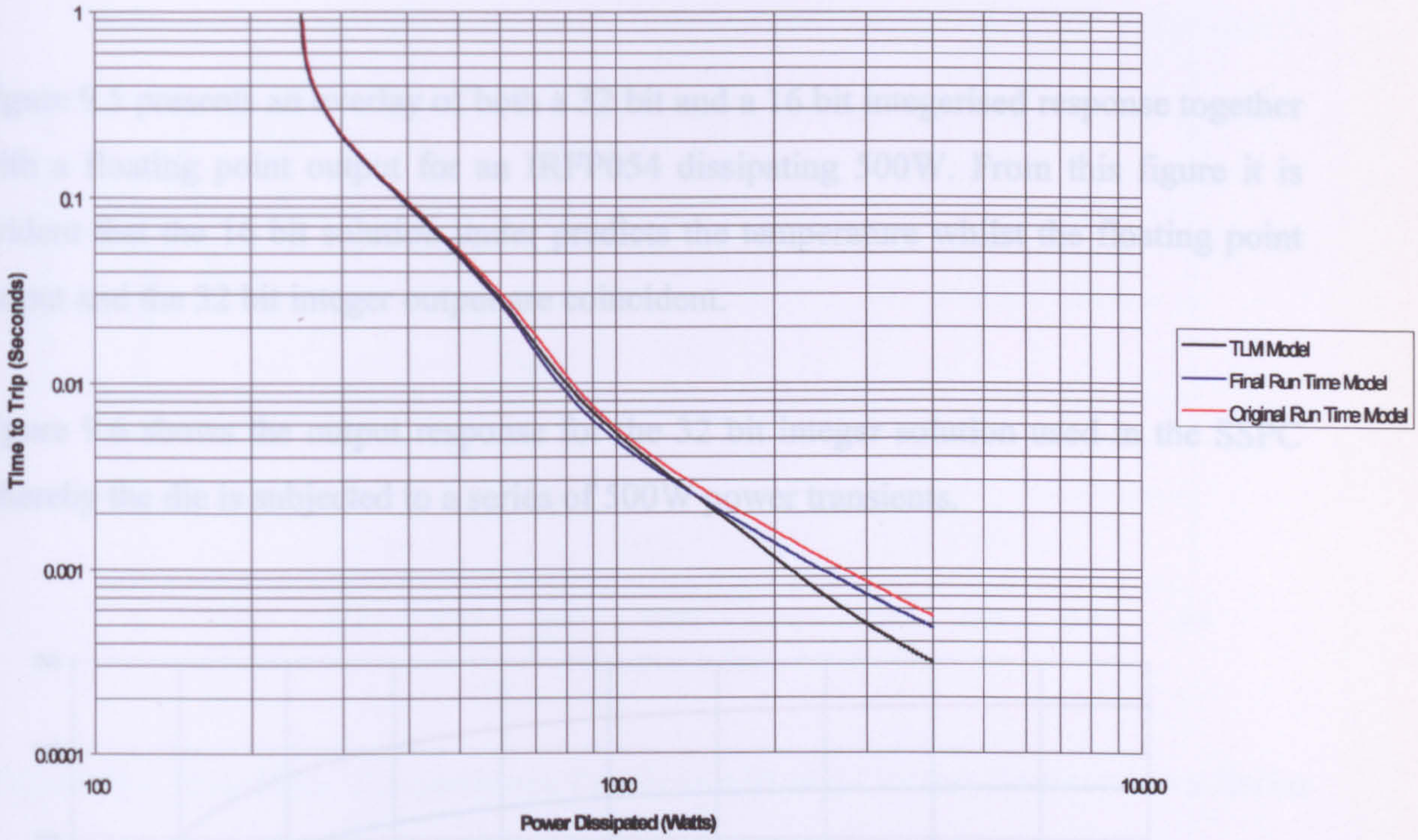


Figure 9.4 Time to Reach 175 Degrees C versus Power Dissipated for IRFP054

As a final consideration with the integerisation issue, both the nodal temperature values and the look-up table contents were represented in an unsigned 16 bit format. This combination offered the quickest execution time owing to the 16 bit architecture of the target microcontroller. Unfortunately evaluation tests of this configuration showed that significant precision was being lost with the result that the calculation was predicting a lower temperature than it otherwise should. As a compromise, it was sufficient to represent nodal temperature values in an unsigned 32 bit format whilst keeping the table contents as a 16 bit number. Using this scheme even if the table contents held only an exponent value this could be added to the nodal temperature without the need to truncate any of its digits.

The final result of this configuration was that the execution time for the temperature prediction algorithm was reduced to 47μs and the maximum error recorded between a floating point model and the run time model was 2.69×10^{-4}%, as such this represented

only a 0.039 Degree C discrepancy for a 500W dissipation after a heating duration of 100ms.

Figure 9.5 presents an overlay of both a 32 bit and a 16 bit integerised response together with a floating point output for an IRFP054 dissipating 500W. From this figure it is evident that the 16 bit solution under predicts the temperature whilst the floating point output and the 32 bit integer output are coincident.

Figure 9.6 shows the output response for the 32 bit integer solution used in the SSPC whereby the die is subjected to a series of 500W power transients.

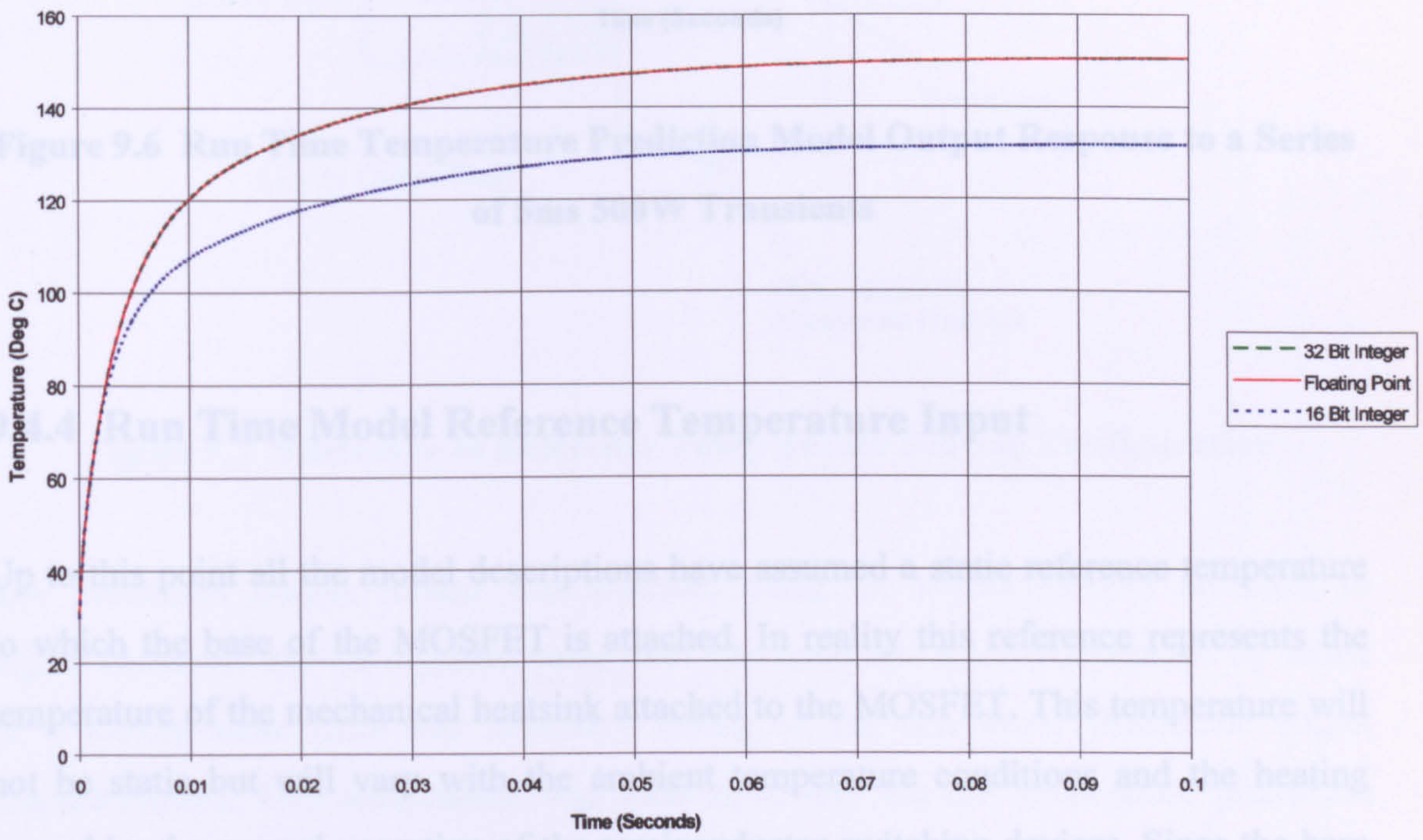


Figure 9.5 Comparison of Floating Point and Integer Model Predictions for an IRFP054 with a Dissipation of 500W Dissipation

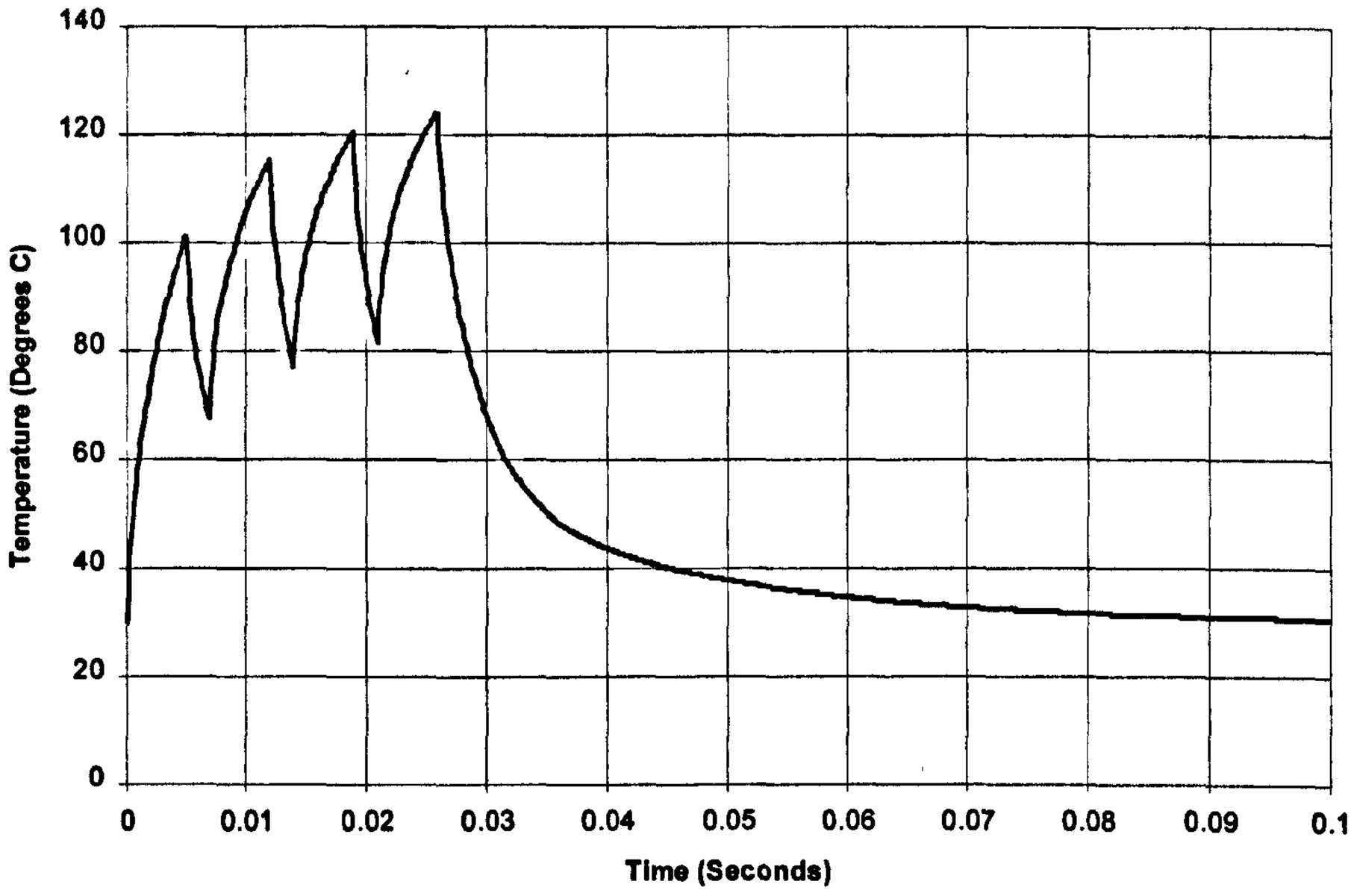


Figure 9.6 Run Time Temperature Prediction Model Output Response to a Series of 5ms 500W Transients

9.4.4 Run Time Model Reference Temperature Input

Up to this point all the model descriptions have assumed a static reference temperature to which the base of the MOSFET is attached. In reality this reference represents the temperature of the mechanical heatsink attached to the MOSFET. This temperature will not be static but will vary with the ambient temperature conditions and the heating caused by the normal operation of the semiconductor switching devices. Since the base temperature is not static, one could determine the highest (worst case) temperature it is likely to attain and use this as the reference in the run time model. However in Chapter 2, it was stated that an attribute of a good protection device is that it should be insensitive as possible to transient current overloads. A solution which relied on using the worst case base temperature would not only have a detrimental impact on this operational goal but would also negate the effort applied to attaining an accurate run

time temperature prediction model. In consideration of this, the approach adopted to overcome the problem was to insert a temperature sensor (thermistor) into the heatsink assembly so that it was in close proximity with the base (copper side) of the MOSFET. Figure 9.7 shows a schematic of this configuration.

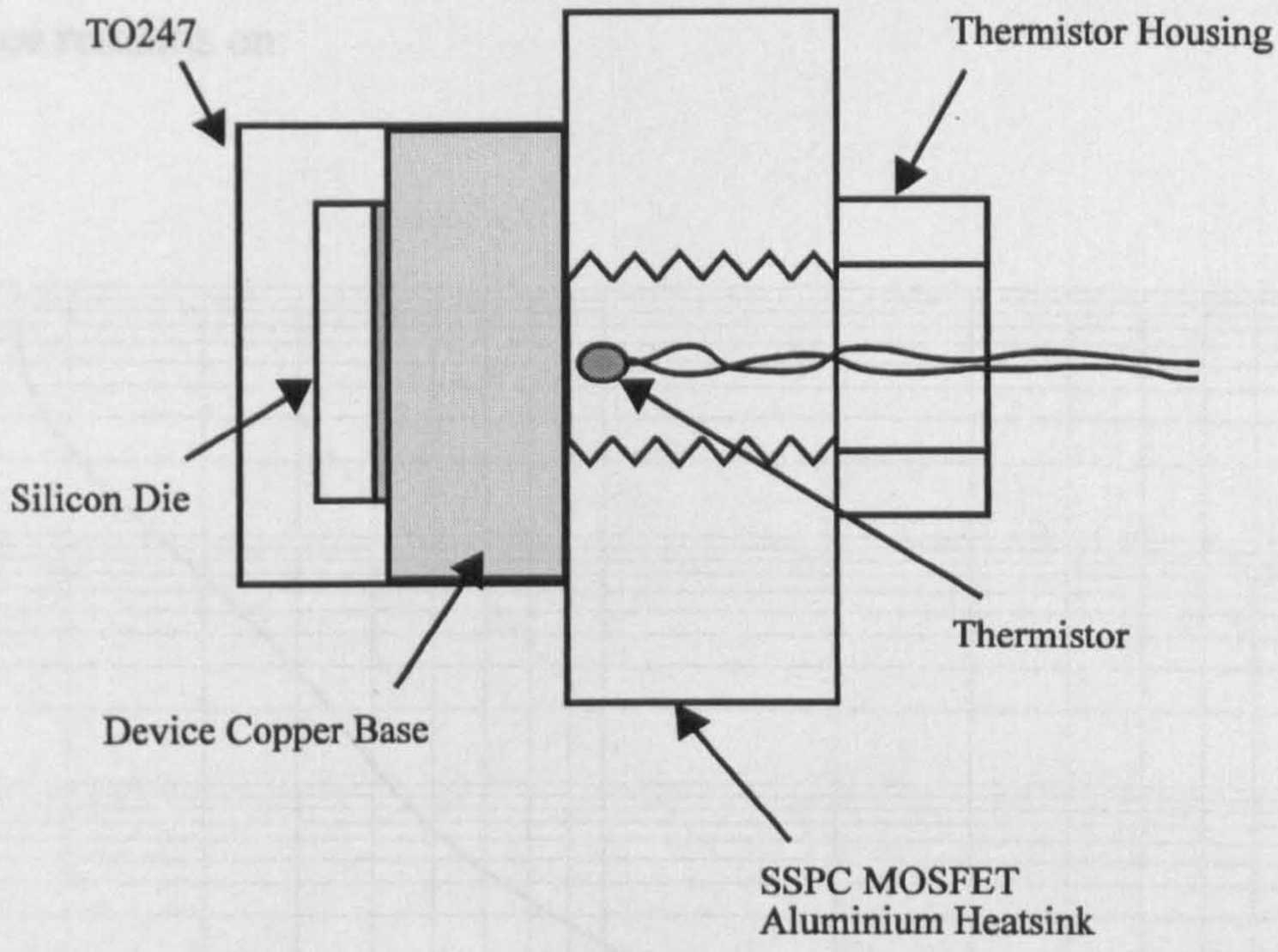


Figure 9.7 Schematic of Reference Temperature Sensing Configuration

The thermistor output voltage was digitised using the microcontroller analogue to digital converter and the digitised value then translated into a real temperature by virtue of a lookup table (this was necessary owing to the non linear thermistor output characteristics). This temperature was then input into the die temperature prediction program and served to provide a reference value from which any temperature rise was calculated. Owing to the fact it was not possible to have direct physical contact with the base of the MOSFET (i.e. the thermistor had a resin coating and was situated approximately 1.6mm from the point of contact) it was considered necessary for the purposes of maintaining temperature accuracy to account for this by modifying the run time model to include part of the heatsink assembly surrounding the thermistor insert. As such, the aluminium heatsink layer was modelled as a continuation of the existing

one dimensional structure to a depth of 3.215mm. This placed the thermistor in the position which would be occupied by a node if the numerical model were extended. Figure 9.8 presents a modified power dissipated versus time to trip curve detailing the acceptable trip band which is introduced by the -40 Degrees C to +70 Degrees C measuring capability of the thermistor insert. From this curve it is evident that the hotter the MOSFET at the beginning of the high power dissipating event, then the shorter the time the device remains on.

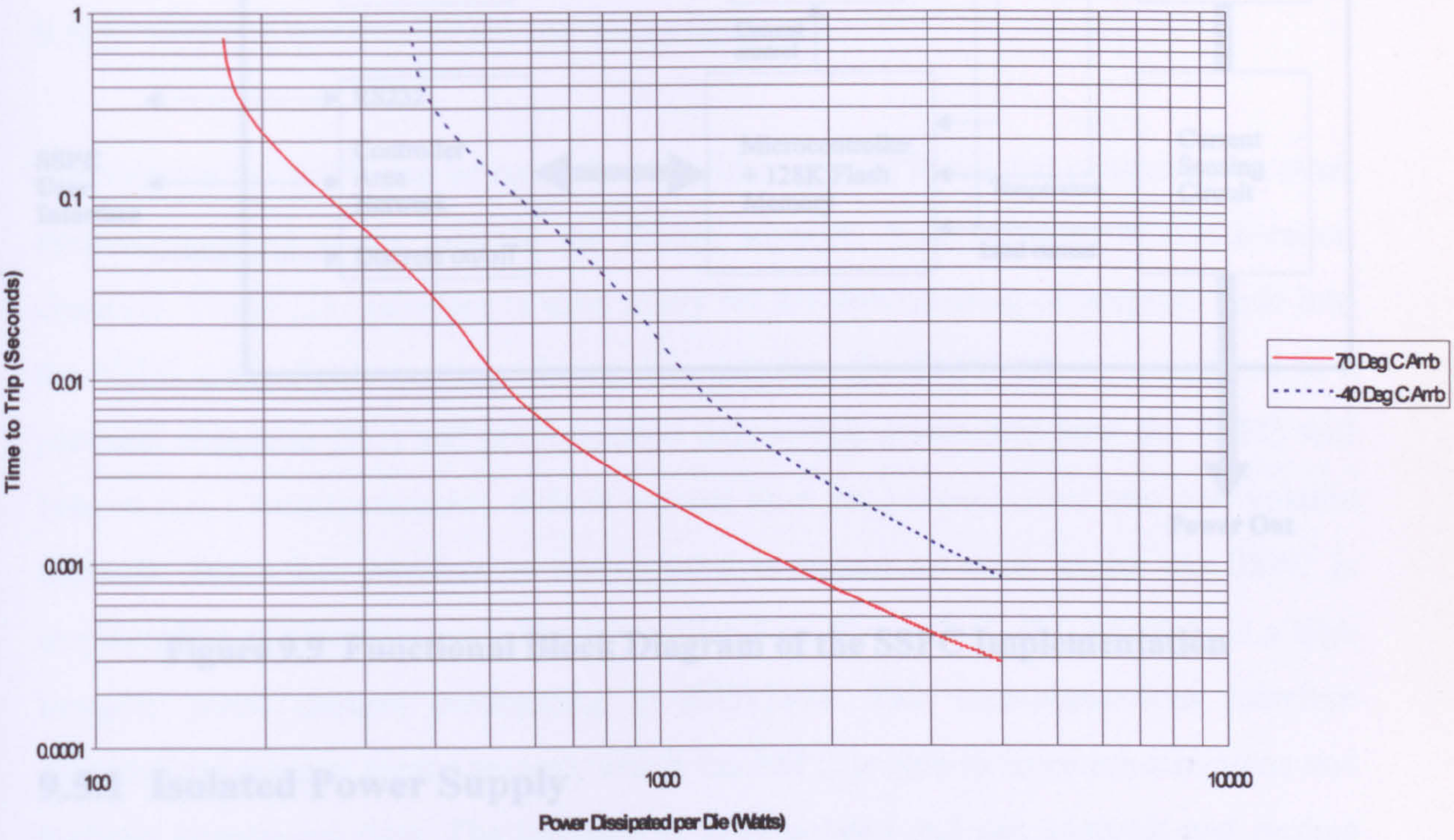


Figure 9.8 The Effect of Reference Temperature Extremes on the Time to Trip versus Power Dissipated Response for an IRFP054

9.5 SSPC Functional Description

This section provides an overview of the functional component blocks which collectively comprise the SSPC implementation. Figure 9.9 shows a schematic of the

SSPC and details the important functional blocks and control relationships between the internal components

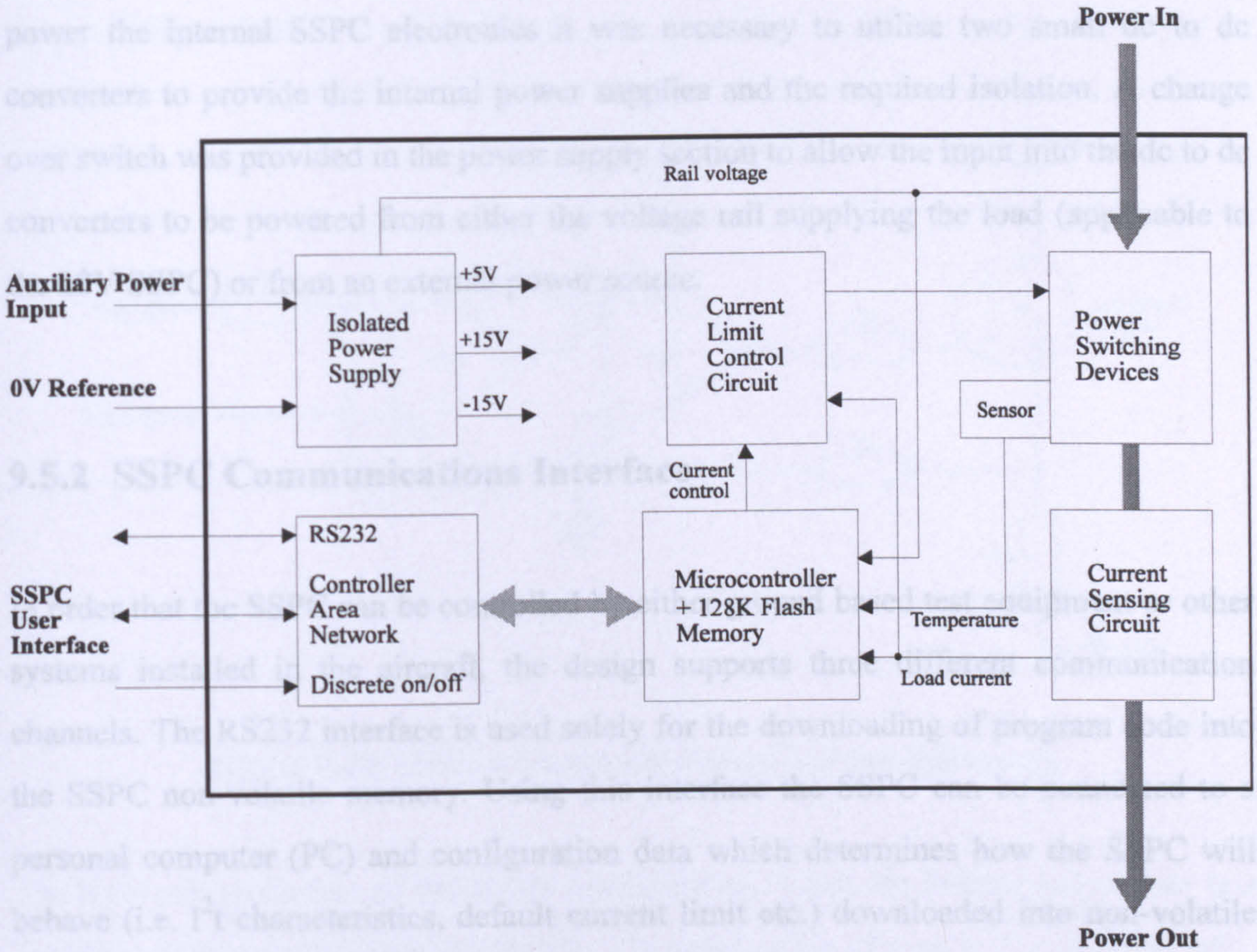


Figure 9.9 Functional Block Diagram of the SSPC Implementation

9.5.1 Isolated Power Supply

One requirement of the SSPC implementation was that it should be capable of powering an electrical load in a high side configuration. This is the usual configuration used in aircraft installations, (i.e. where the airframe itself is used as a common ground (0V)). In order to achieve this requirement it was necessary to reference most of the SSPC internal electronics to the high side of the electrical load. With this scheme when the SSPC is turned off and no load current is flowing the internal electronics will very nearly be referenced to the aircraft 0V by virtue of the resistance path of the electrical load itself. By contrast when the SSPC is turned on and conducting load current, the

reference voltage will now be very close to that of the voltage rail powering the load. To accommodate this floating reference and achieve a stable internal power supply to power the internal SSPC electronics it was necessary to utilise two small dc to dc converters to provide the internal power supplies and the required isolation. A change over switch was provided in the power supply section to allow the input into the dc to dc converters to be powered from either the voltage rail supplying the load (applicable to the 28V SSPC) or from an external power source.

9.5.2 SSPC Communications Interface

In order that the SSPC can be controlled by either ground based test equipment or other systems installed in the aircraft, the design supports three different communication channels. The RS232 interface is used solely for the downloading of program code into the SSPC non-volatile memory. Using this interface the SSPC can be connected to a personal computer (PC) and configuration data which determines how the SSPC will behave (i.e. I^2t characteristics, default current limit etc.) downloaded into non-volatile memory. Since this interface is non-isolated it cannot be used whilst the SSPC is connected to an electrical load. The Controller Area Network (CAN) interface is a high integrity serial channel conforming to ISO11898. This communications interface provides the primary means through which the SSPC is able to receive instructions and transmit operational data. The interface is opto-isolated and can transmit and receive serial data at speeds of up to 1M bits/sec. The discrete on/off input allows a user to turn the SSPC on or off in absence of a CAN interface connection. This discrete is opto-isolated so it may be used when the SSPC is powering an electrical load.

9.5.3 Current Limitation

Chapter 5 provided details of how excessive drain source current in a commercial MOSFET can cause its destruction. In order to avoid this situation the SSPC design

utilised a current limiting circuit which had the task of containing the magnitude of any overload fault current to an acceptable level. A schematic of the configuration used is shown in Figure 9.10

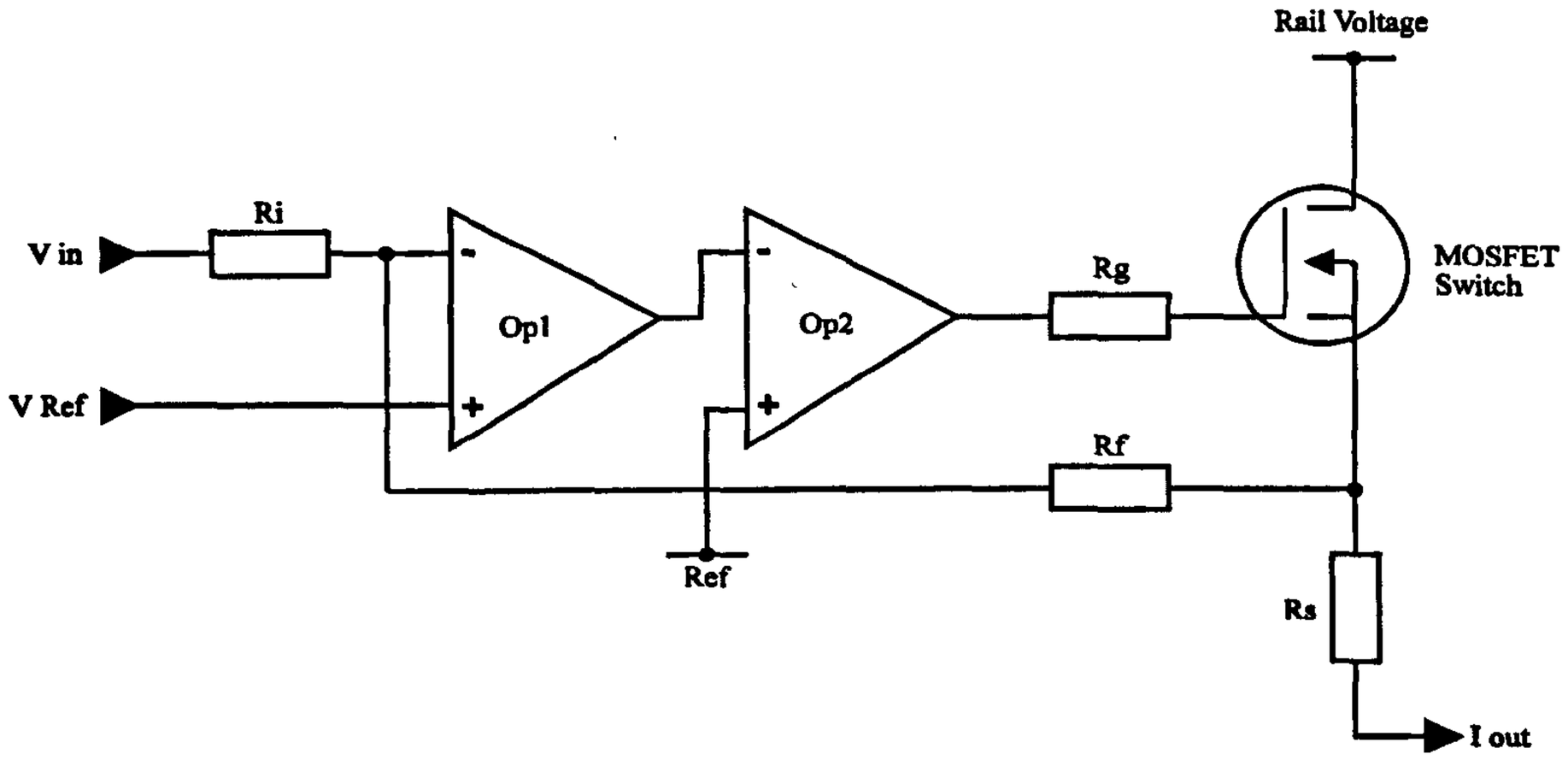


Figure 9.10 SSPC Current Limitation Circuit Schematic

The most salient feature of the above configuration is that the current output *Iout* is a function of the variable input voltage *Vin.* The relationship of *I out* to *V in* is given by:

$$Iout = \frac{\left(Vref \times \left(1 + {Rf}/{Ri}\right) - \left(Vin \times {Rf}/{Ri}\right)\right)}{Rs} \qquad \text{- (9.6)}$$

Where *Rf, Ri* and *Rs* are resistor values in ohms and *Vref* is a static reference voltage.

The voltage *Vin* is derived from a microcontroller pulse width modulated output, and as such, its adjustment is under the direct control of the SSPC embedded software. Using this facility the SSPC is able to raise or to lower the current limit dynamically to follow the profile of the electrical load current demand. If the load characteristics are subject to an inrush condition the current limit is raised to accommodate the inrush duration and then is progressively lowered to a value reflecting the steady state load current demand.

This mechanism serves to reduce the impact of a short circuit fault on the power rail supplying the SSPC since the fault current will be as small as possible without affecting the normal load operation. Likewise, the transient insensitivity of the SSPC will also be improved since under short circuit fault conditions the power dissipation in the MOSFET switching element will be reduced, thus allowing a longer remain on time. Figure 9.11 shows the operation of this scheme whereby the current limit tracks the profile of the inrush current into an electrical load.

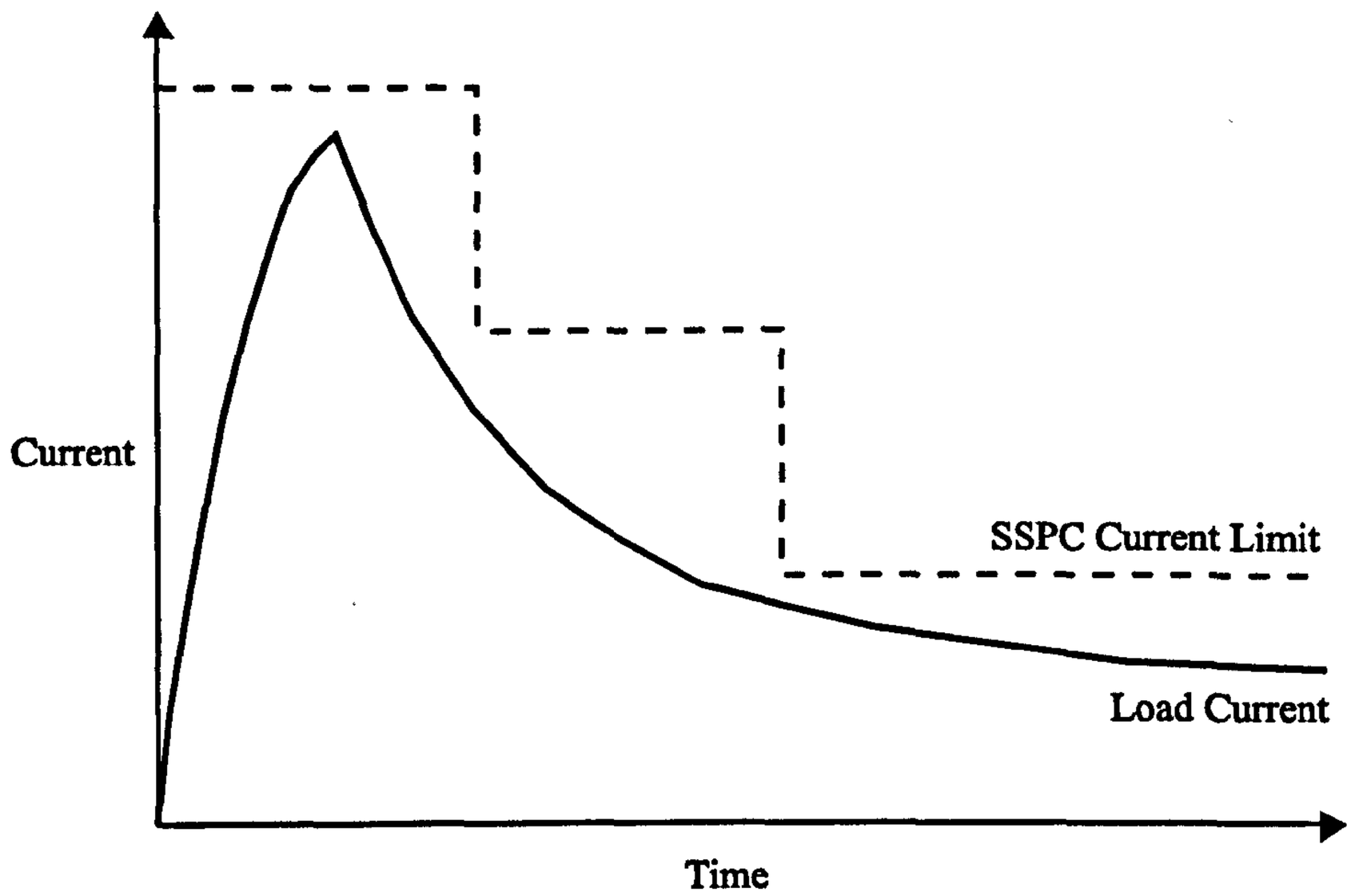


Figure 9.11 Operation of Dynamic Current Limitation

An important issue with the current limiting circuit is that in order to avoid a large overshoot in fault current the speed of response should be as fast as possible. The major constraint on how quickly the circuit can limit the fault current is how rapidly it can discharge the MOSFET gate capacitance. The SSPC was constructed to accommodate up to 8 MOSFET devices. Each MOSFET presents a gate capacitance of about 5000pF. To discharge such a relatively large capacitive load rapidly the MOSFET's are collectively controlled via a buffer amplifier with a 1.5A output drive capability. The result of this configuration is that the MOSFET devices can be switched from saturation into a linear mode of operation in approximately 400ns.

One problem associated with the current limitation philosophy is that whilst the MOSFET is fully saturated its temperature coefficient is positive. As discussed previously in Chapter 3, this phenomenon means that any paralleled devices will be forced to share current equally. When the MOSFET is in its linear region of operation however, as would be the case when limiting fault current, the temperature coefficient becomes negative [86]. Under these conditions paralleled MOSFET's might not share current equally and assumptions made about the power dissipation in each device will no longer be valid i.e.

$$Power\ Dissipated\ per\ Device = \frac{Total\ Power\ Dissipated\ in\ Switching\ Element}{Number\ of\ Devices\ Paralleled}.$$

From the manufacture's catalogue [35] the transfer characteristics ($I_D = f(V_{GS})$) provided for each of the two MOSFET devices used in the SSPC implementation reveal the drain current at which the temperature coefficient goes from negative to positive (the zero temperature coefficient point 0TC) to be 45A for the IRFP054 and 23A for the IRFP450.

A solution based on configuring the current limit to always be in excess of these points would not be a viable option since raising the limit to a sufficiently high level would negate many of the advantages of having a current limitation facility. Similarly reducing the number of MOSFET's utilised in the SSPC in order to boost the current density in each device would have the detrimental effect of increasing the conduction voltage drop across the SSPC and reducing the SSPC's insensitivity to transient overloads.

The problem has previously been highlighted by Fachinetti [21] in the description of a SSPC for spacecraft applications but no comments were offered for minimising the impact of the condition. Severns [42] however analyses the problem and recommends thermal coupling between devices in order to reduce the effects of devices which have a higher temperature commanding more of the load current owing to the reduction of threshold voltage. Similarly he recommends adding a small resistor to each MOSFET

source output so as to introduce a negative feedback term i.e. as I_D increases the V_{GS} is reduced so reducing I_D. In consideration of these points effort was made to ensure the MOSFET's used in the SSPC design were thermally coupled through both the heatsink and through the case. Low value resistors were also placed on the source output of each MOSFET. As a useful feature the voltage across each of the source resistors was monitored by the multiplexed input of the microcontroller analogue to digital converter. This gave the capability of determining the current balance in each of the switching elements. Although tests conducted using this facility determined that each device returned an identical digital reading, indicating good current sharing, as an added protection feature it was decided to limit the duration that the switching devices could remain in their linear region to one second. The rationale behind this decision was based on the fact that no normal SSPC operation in an aircraft environment would require current limitation in excess of one second. Therefore, if this situation did occur it could be treated as an electrical load fault.

9.5.4 Current and Voltage Sensing

The current sensing circuit utilised an in line resistor to provide a voltage proportional to load current. This voltage is then amplified and directed into one of the microcontroller analogue to digital converter inputs. Similarly the voltage across the switching elements is attenuated with a simple resistive potential divider and then input into another of the conversion channels. By multiplying these two inputs together it is possible for the microcontroller to determine the power dissipation in the SSPC switching devices. One important point to note regarding this scheme however, is that the period between successive samples is 70μs. As a consequence, short power transients which fall between these sample points will be undetected by the microcontroller. In the unlikely event of a continuous train of such pulses going undetected this eventuality could cause significant die heating which would not be resolved by the temperature prediction algorithm. The remedy for this situation was to incorporate into the current and voltage analogue to digital converter input signals a

simple resistor capacitor network with a time constant of 14μs. This simple integrator provides the memory component whereby short transients are translated into a dc offset which can then be detected by the subsequent analogue to digital converter sample.

9.5.5 SSPC Construction

The electrical contents of the SSPC were divided between two circuit boards. One of the circuit boards accommodated the microcontroller, the non-volatile memory and the communication components. The other circuit board contained the power MOSFET's, the internal power supplies and the current limitation control circuitry. The boards were arranged within the SSPC case assembly so that the microcontroller board was mounted on top of the board containing the power components. The two boards were then connected via a flat wire ribbon and physically separated within the enclosure with a mild steel plate (an assembly diagram is presented in Appendix 9). The philosophy of this arrangement was twofold; To reduce the effects of radiated electrical noise from the power section interfering with sensitive digital electronics. To safely contain any debris from the MOSFET power switches should one of the devices be destroyed as a result of an uncontrolled high power overload.

Figure 9.12 and Figure 9.13 shows photographs of the SSPC microcontroller module and the power switching module.

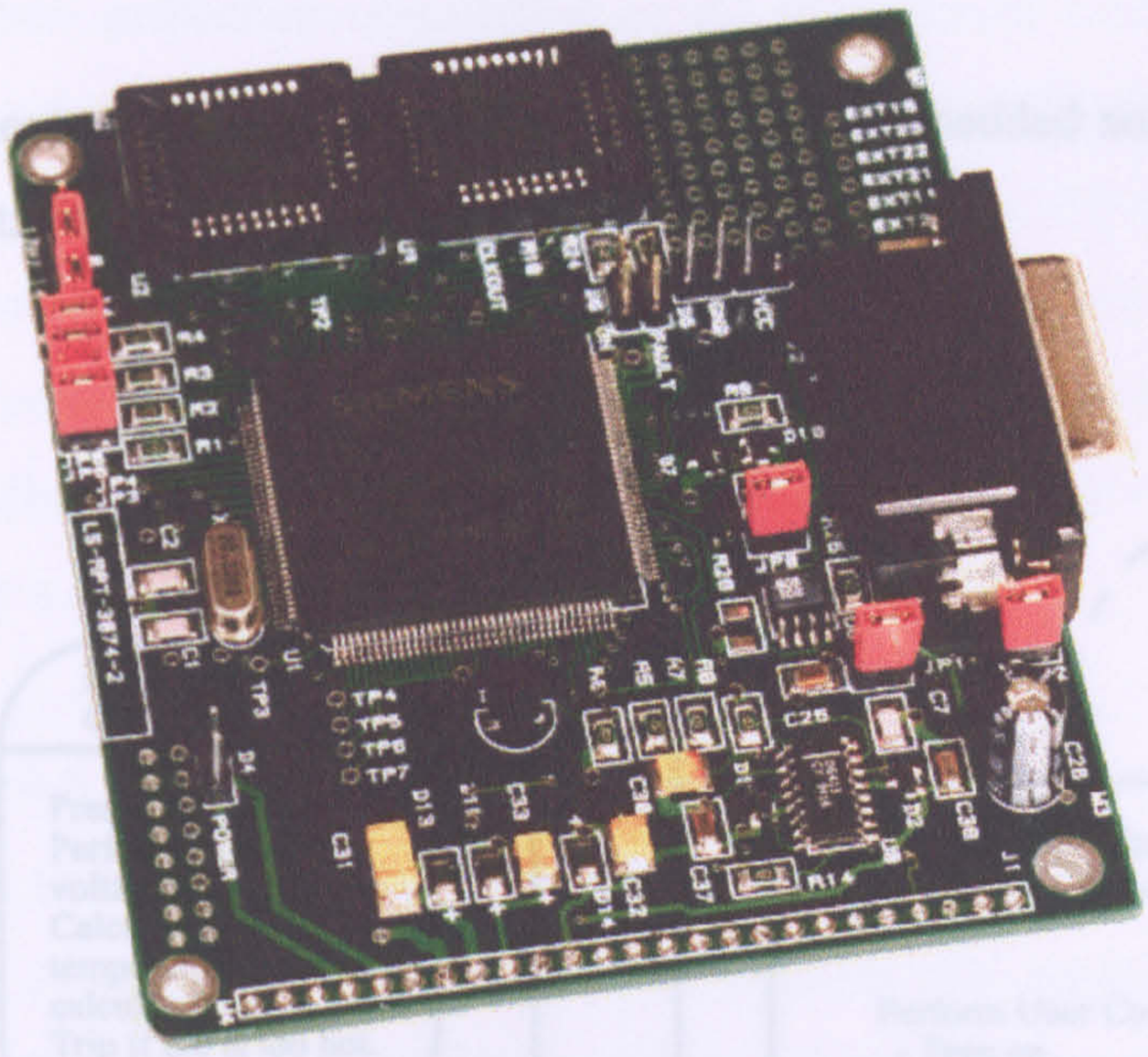


Figure 9.12 Photograph of the SSPC Microcontroller Module

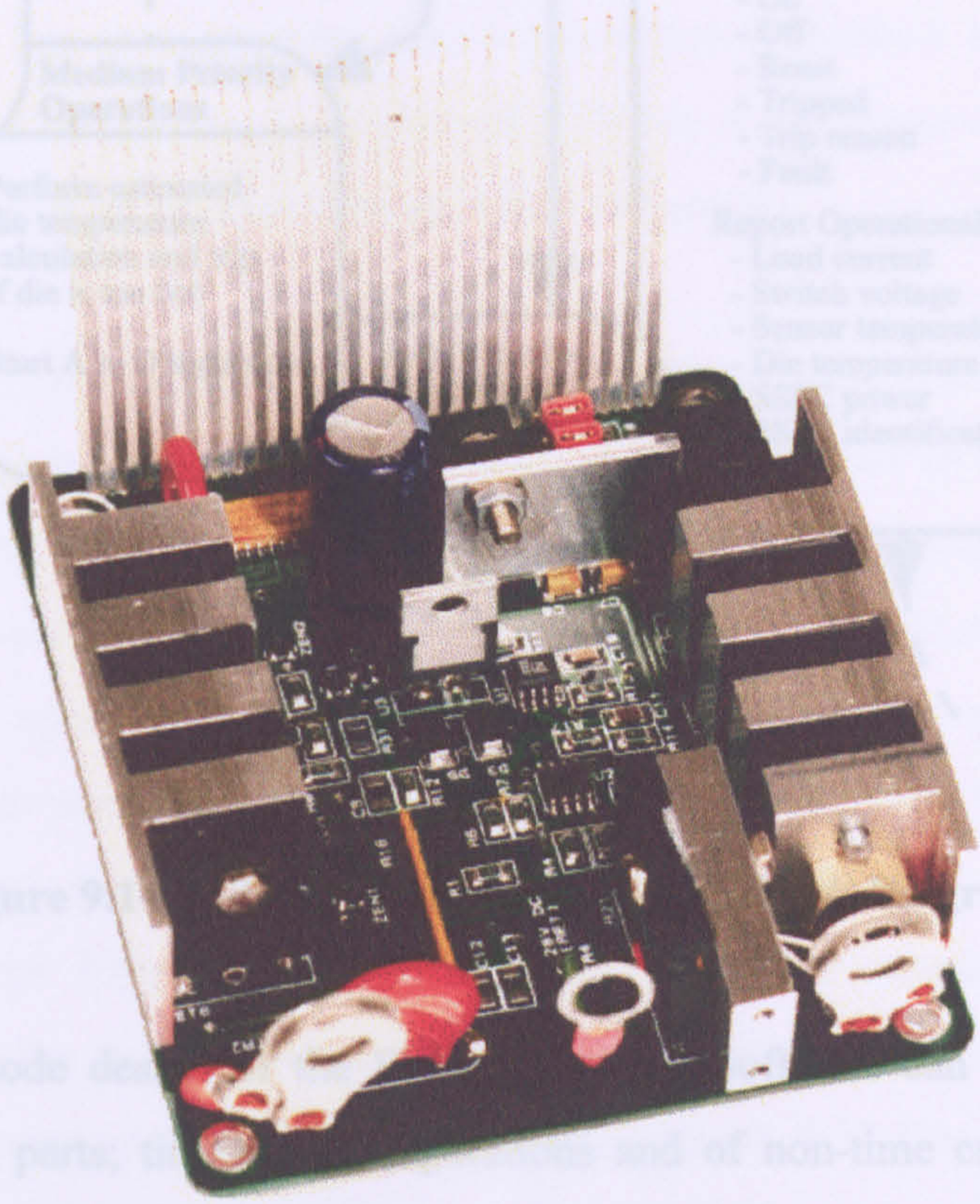


Figure 9.13 Photograph of the SSPC Power Switching Module.

9.6 SSPC Embedded Software Design

Figure 9.14 presents a functional block diagram of the embedded software used in the SSPC implementation.

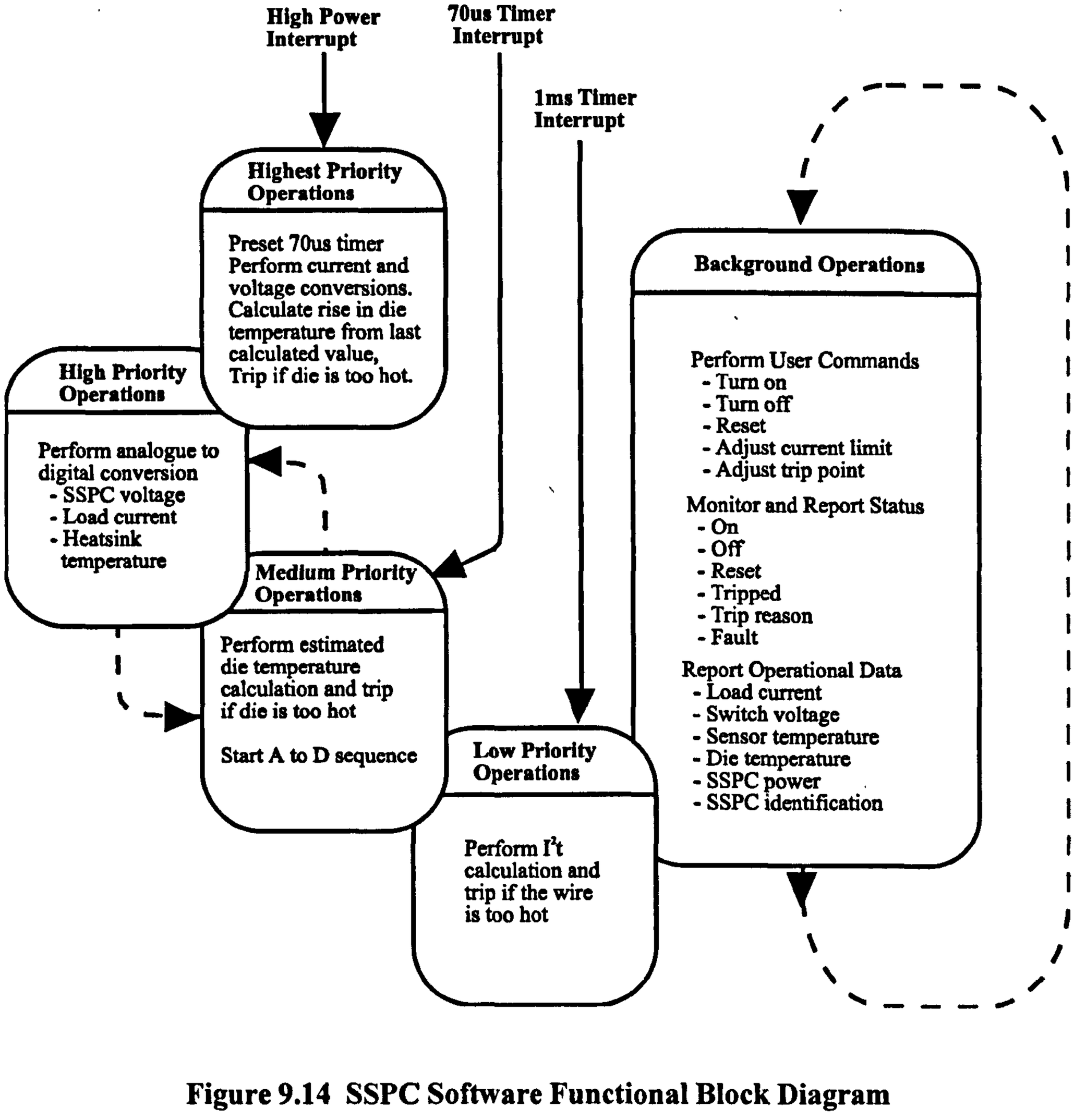


Figure 9.14 SSPC Software Functional Block Diagram

The operational code design of the SSPC embedded software can be categorised as consisting of two parts; time critical operations and of non-time critical background functions. Time critical operations are those which are required to be performed at regular intervals. If this is not so, the output of the operation will be invalid. Time

critical operations are also associated with ensuring the integrity of either the SSPC (i.e. the die temperature prediction calculation) or the downstream load wire (i.e. the I^2t calculation). Non-time critical background operations are those functions which can be performed when the microcontroller is not processing a time critical operation. From Figure 9.14 it can be seen that each of the time critical operations has an associated priority. This is possible as each time critical function is invoked as an interrupt service routine. The SAB167CR microcontroller offers the facility that an interrupt may itself be interrupted by a service routine with a higher priority rating.

The function which continuously performs the die temperature estimation is invoked every 70μs from an on chip interval timer, the actual time this function takes to execute is 46μs, leaving 24μs for remaining tasks. One point to note regarding this routine is that it instigates the analogue to digital conversion of the input parameters required for the protection operations. The conversion routine has a higher priority than the die temperature estimation process and as such interrupts the calculation in order to transfer conversion results into memory every time a conversion is finished. In this way the die temperature estimation routine is interleaved with the A to D conversion process and always has a complete set of input data on which to operate.

The highest priority operation is the high power interrupt which occurs when a larger than normal voltage is dropped across the switching element; this indicates the SSPC is in current limitation. This interrupt service routine is necessary owing to the fact with a 70μs period the worst case delay between an event taking place and the temperature rise being predicted is approximately 127μs. This means the die temperature could rise by 16 Degrees C under worst case power conditions and this rise would be undetected. The interrupt performs a reset operation on the 70μs period clock and then samples both voltage and current followed by a temperature prediction calculation. This action ensures the delay after the start of event is maintained within the 70μs calculation period and as such the worst case undetected temperature rise is 9.33 Degrees C (this rise is accommodated by the 10 Degrees C tolerance applied to the trip temperature) .

The background operations are configured into a never ending loop so as to always be performed whilst the SSPC is powered. These functions are generally associated with the carrying out of command instructions and reporting status/statistical information back via the serial controller area network bus.

9.7 SSPC Testing

The testing strategy used for the SSPC implementation primarily focused on performing a comparison between the theoretical 'model' trip response and the actual trip response achieved by the SSPC for comparable levels of power dissipation and ambient temperature. In addition to this exercise the testing phase also included tests to examine the limits of the design and ensure the SSPC could switch, without incident, representative aircraft loads.

9.7.1 SSPC Test Configuration

The SSPC test configuration was similar to that previously utilised in Chapter 4 to test Smartfet products. The general test strategy once again focused on subjecting the SSPC to a current overload by creating a short circuit across the electrical load it was powering. Figure 9.15 details a schematic of this general test configuration.

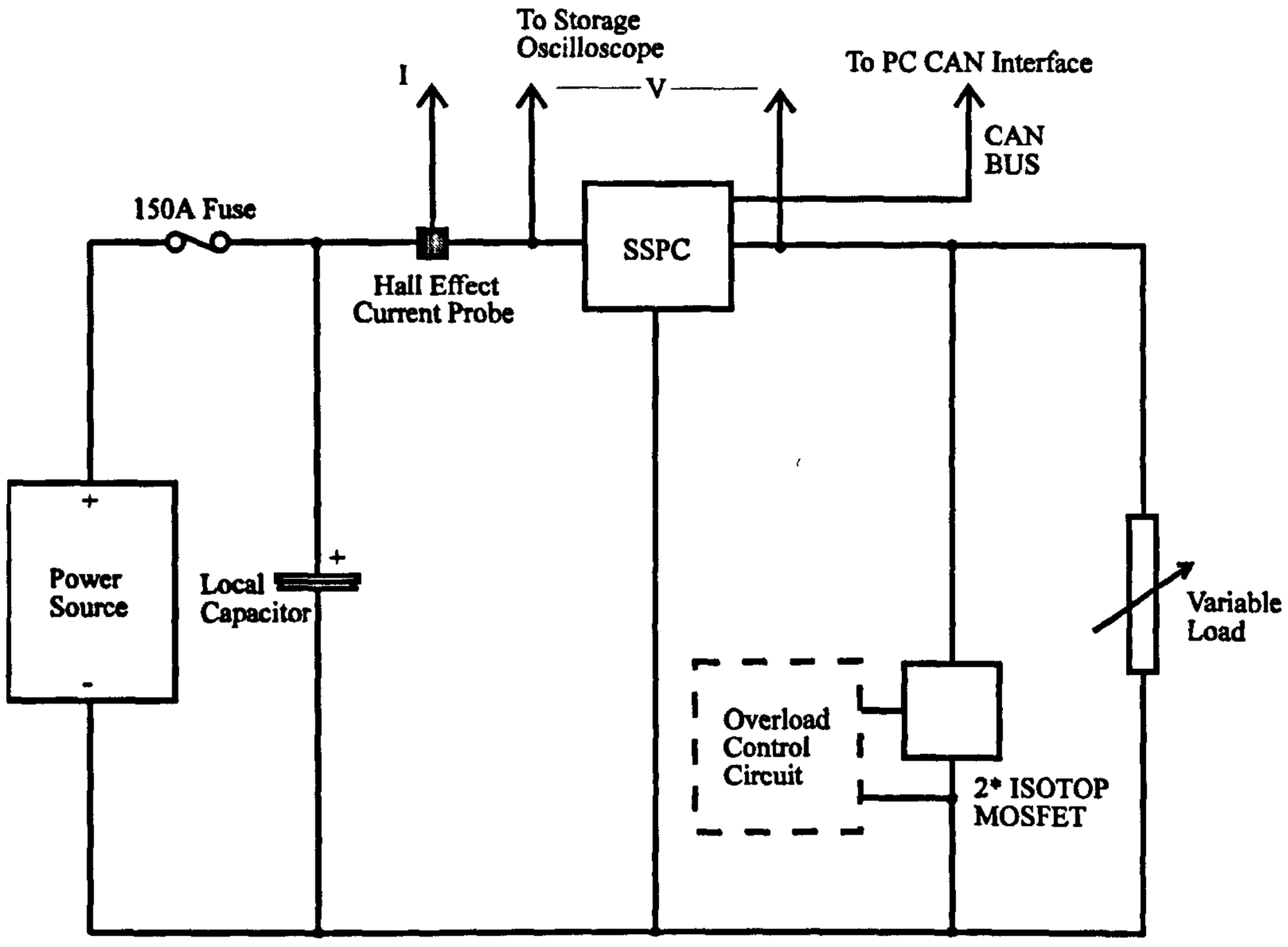


Figure 9.15 Schematic of SSPC Test Circuit

It should be noted that although the general format of the test circuit given in Figure 9.15 is valid for both 28V and 270V SSPC's, however it was necessary to interchange certain equipment depending on which SSPC was the subject of examination.

For the 28V SSPC tests the power source was two series wired lead acid batteries giving a nominal 26V supply >200A capability. The capacitors local to the SSPC had a combined value of 50mF and a rating of 35V (this was required to compensate for the inductance and series resistance of the power feeds during high current pulse experiments). The variable load was a 6Ω 1.5KW rheostat and the modules which could short out this load were two STE25N06 250A ISOTOP MOSFET's.

The power source for the 270V test configuration used the full wave smoothed and rectified output of a 13 Amp mains powered autotransformer. The capacitors local to the SSPC had a combined value of 2.8mF and a rating of 250V (this voltage represented a compromise since the capacitance provided by 400V rated devices was significantly

lower than the 250V parts). The variable load was a 50Ω rheostat which was implemented through five, 10Ω 500W rheostats wired in series. The modules which could short out this load were two STE53NA50 53A ISOTOP MOSFET's. A control circuit provided the facility for these ISOTOP modules to be turned on for a precise time duration in the range 10μs to 1 second (simulating transient current overload faults). Alternately the ISOTOP modules could be turned on fully for an indefinite period. Current measurements were made using a hall effect current probe. This output, together with the voltage across the SSPC, was then recorded on a digital storage oscilloscope. Also crucial to any experiments were the recorded output from the SSPC itself. The SSPC was programmed to output via the CAN interface its value of measured load current, voltage across the internal switching elements, temperature recorded from the temperature sensors and predicted die temperature. These output values were displayed on a personal computer which had a CAN interface card installed. As an added feature to assist with the testing activity, the SSPC software also included a utility which took a snapshot of the calculated power dissipation in the switching elements and the predicted die temperature every time the SSPC tripped as a result of an overload. This facility provided a means of cross checking the level of dissipated power determined by the SSPC with that of the power extrapolated from the oscilloscope voltage and current trace.

9.7.2 Power Dissipated Versus Time to Trip Test Results

The purpose of this test was to determine the accuracy of the trip response for a known level of dissipated power. The method of the test was to first configure (via the CAN interface) the level of the SSPC current limit and then turn the device on so that it supplied a nominal load current. The SSPC was then subjected to a sustained current overload by applying a short circuit across the load. The time taken from the start of this short circuit to the time where the SSPC trips was then recorded by virtue of the oscilloscope voltage and current trace. The Figures 9.16 and 9.17 display the typical current and voltage waveform obtained from the SSPC whilst performing the overload

tests (note the SSPC was configured with 2 MOSFET's hence the power dissipated in each die will half that indicated by the voltage and current product).

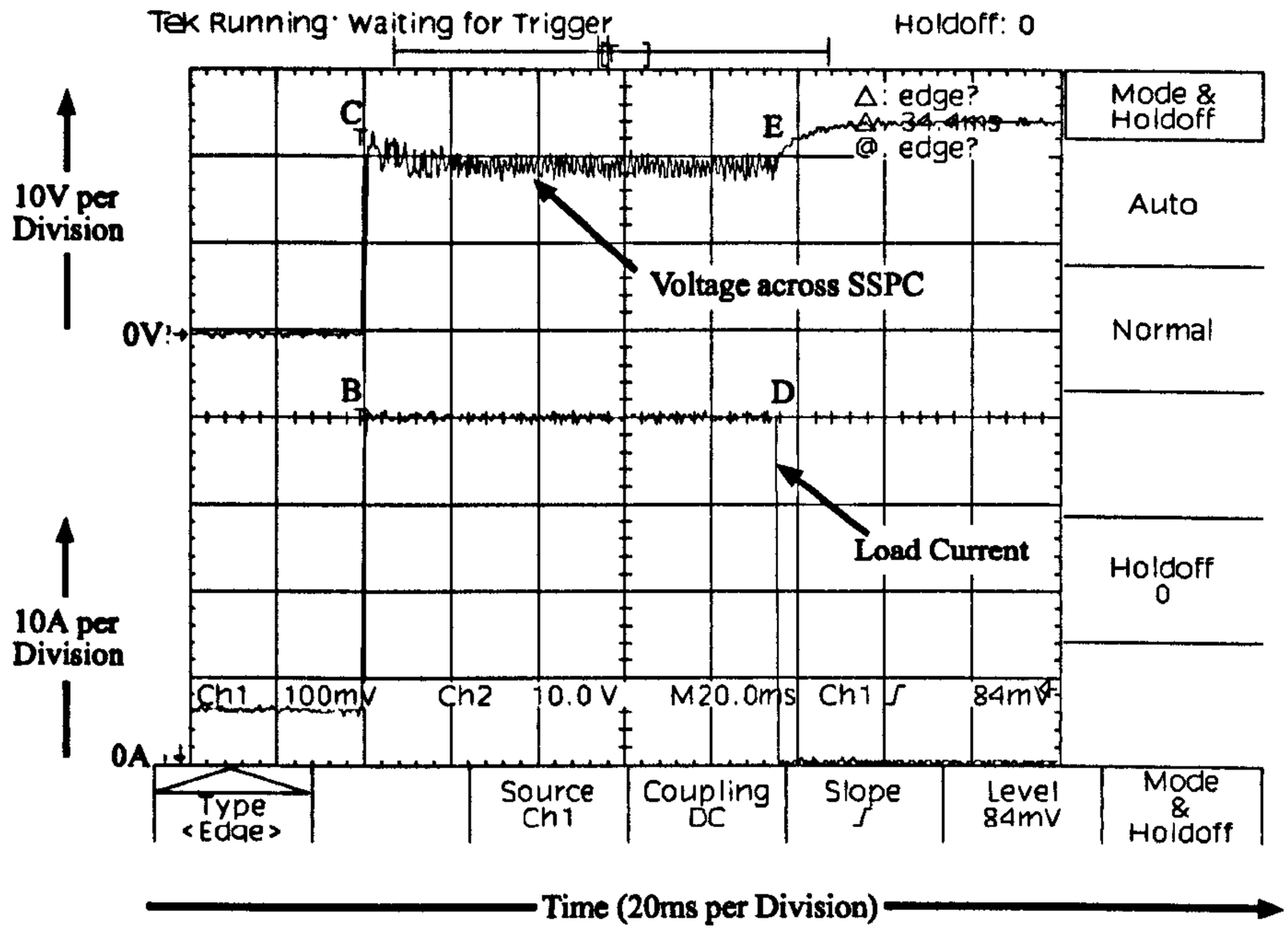


Figure 9.16 Waveforms Showing Current Limitation @40A and Trip Condition

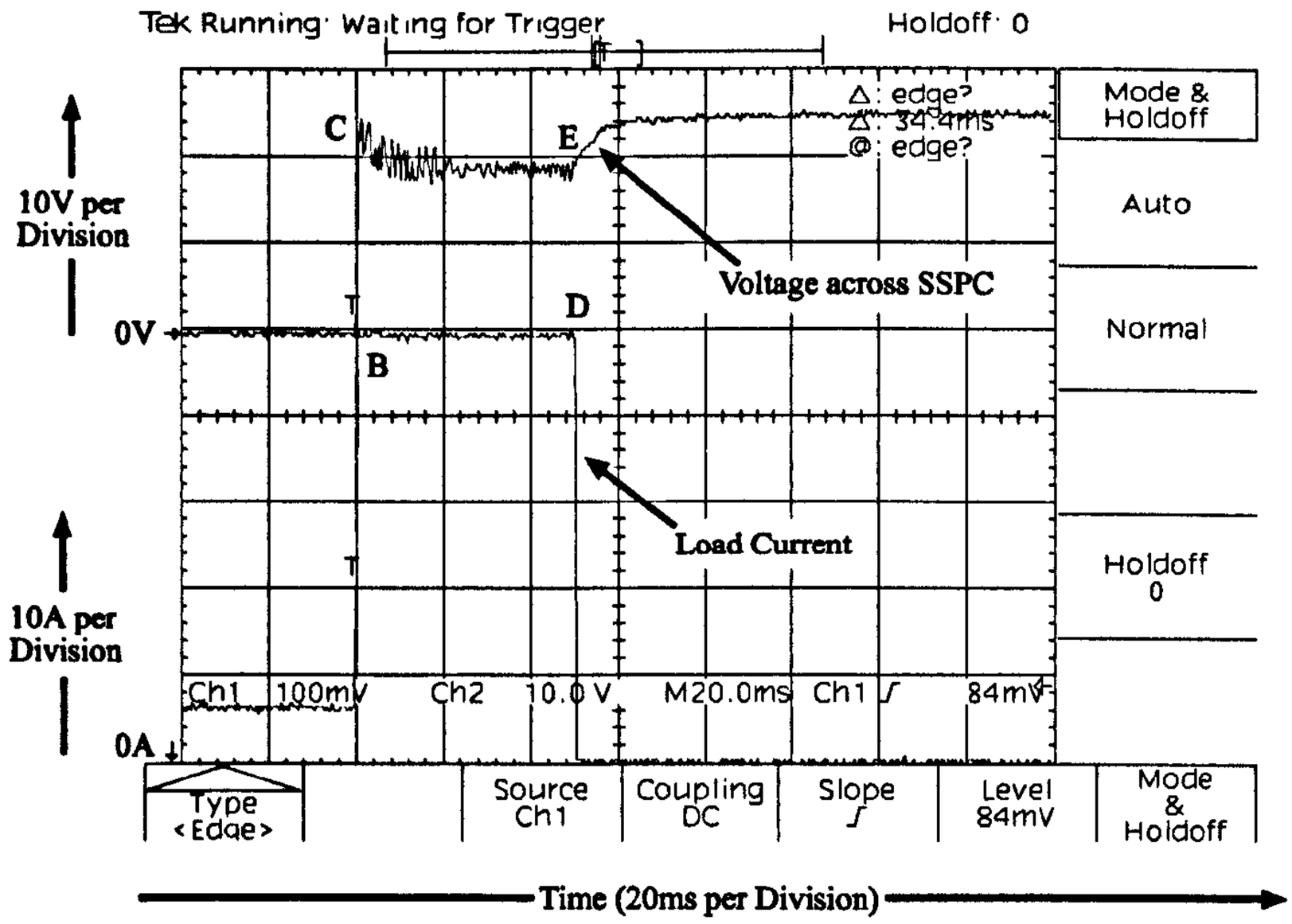


Figure 9.17 Waveforms Showing Current Limitation @50A and Trip Condition

From the oscilloscope waveforms it can be observed that whilst the SSPC is normally delivering current to the load the voltage across it is very small. Once the overload begins however, the voltage rises rapidly (this event is indicated by point C) so that the entire supply potential is dropped across the SSPC. As a simultaneous event, the fault current is being maintained at a constant level by the SSPC control circuitry (see point B). The large power dissipation resulting from this condition eventually causes the SSPC to disconnect the load when the predicted MOSFET die temperature exceeds the predefined limit. The current then falls to zero whilst the voltage is maintained across the SSPC (as indicated by points C and D).

Figure 9.18 presents the test results obtained by performing a series of tests similar to those described above.

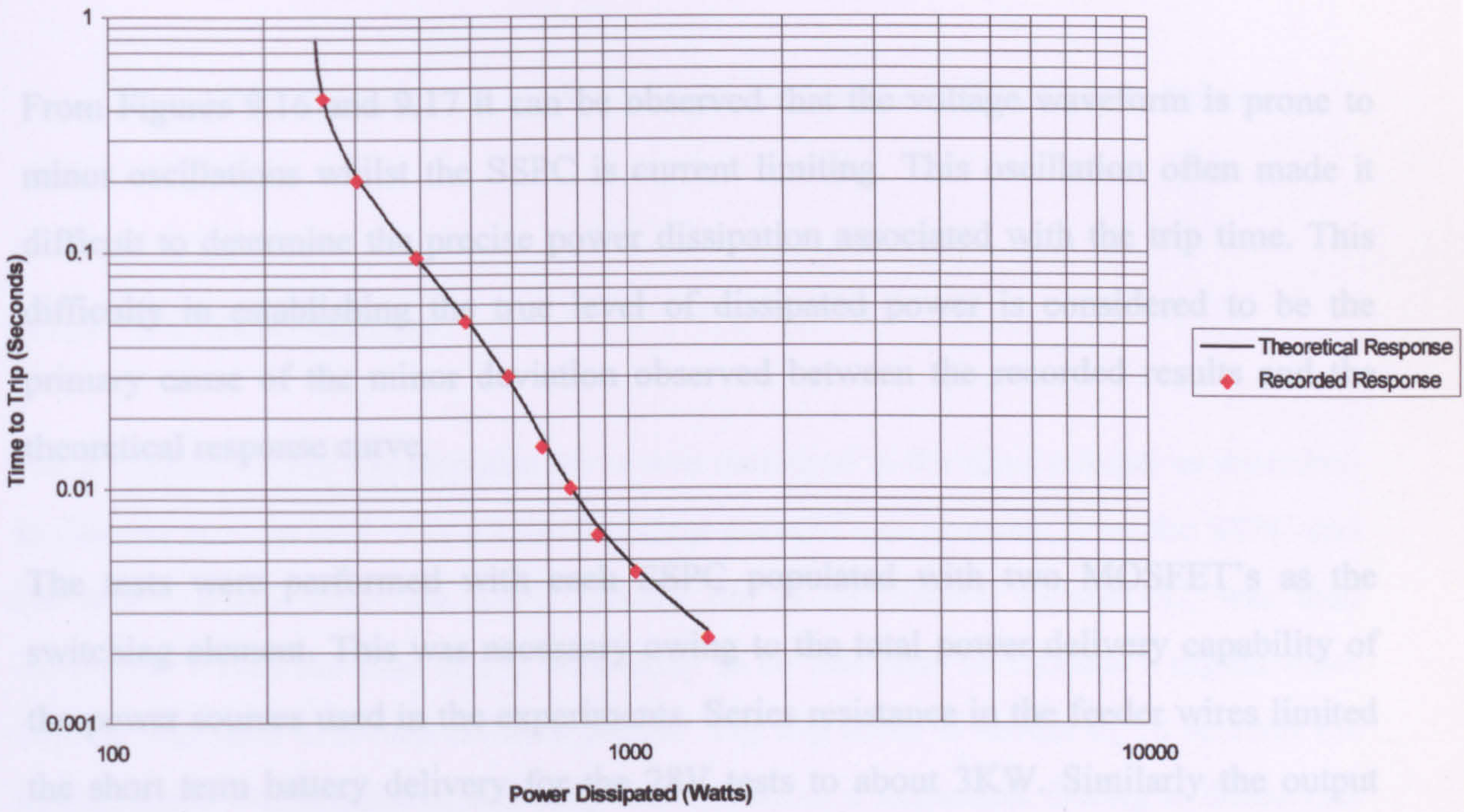


Figure 9.18 Comparison of Theoretical and Actual Trip Times

From Figure 9.18 it can be observed the values recorded from the experiments correspond reasonably closely with the predicted response curve. There are however a number of issues concerning these results that require comment.

In order to expedite the tests the thermal sensor temperature was ignored and the SSPC embedded software modified so that the reference temperature input was always 25 Degrees C. This action avoided having to wait for the temperature to stabilise to that of the reference temperature used in the theoretical response curve after each test.

The power dissipation in the SSPC during each test was extrapolated from the current and voltage waveforms obtained from the oscilloscope trace. In addition, the SSPC was also programmed to transmit the value of dissipated power it calculated throughout the course of the test. It should be noted however that the value obtained from the SSPC was to act only as a guide owing to the limited speed of sampling.

From Figures 9.16 and 9.17 it can be observed that the voltage waveform is prone to minor oscillations whilst the SSPC is current limiting. This oscillation often made it difficult to determine the precise power dissipation associated with the trip time. This difficulty in establishing the true level of dissipated power is considered to be the primary cause of the minor deviation observed between the recorded results and the theoretical response curve.

The tests were performed with each SSPC populated with two MOSFET's as the switching element. This was necessary owing to the total power delivery capability of the power sources used in the experiments. Series resistance in the feeder wires limited the short term battery delivery for the 28V tests to about 3KW. Similarly the output impedance of the auto-transformer used to generate the 270V dc supply coupled with the 50Hz charging rate resulted in the output voltage collapsing rapidly for load currents greater than 10A.

Figure 9.19 shows an example trace of where the SSPC operating at 250V was subjected to a short circuit (note SSPC current limit was set at 20A).

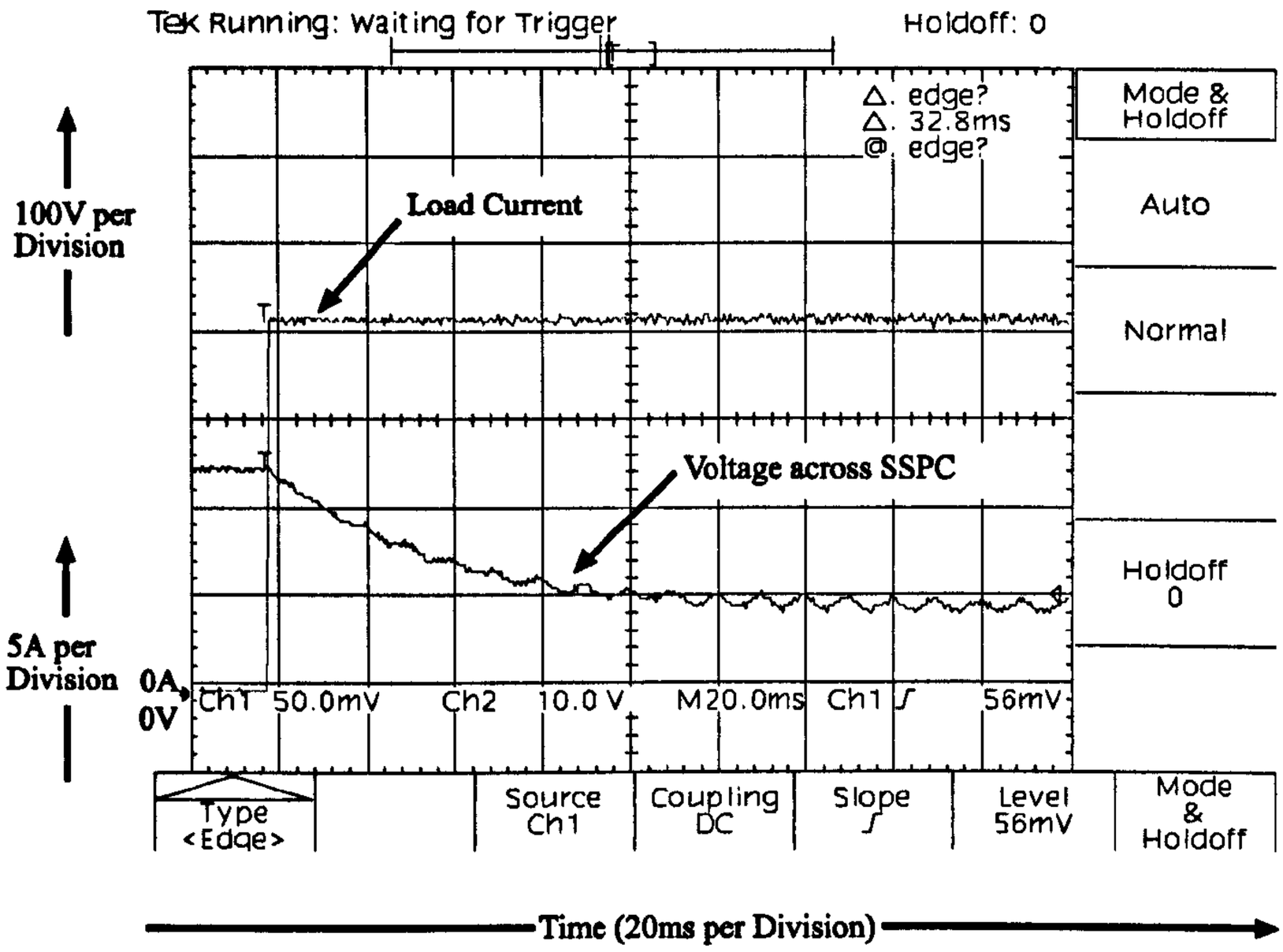


Figure 9.18 Example of 270V Collapse Under Short Circuit Conditions

9.7.3 I^2t Test Results

The I^2t portion of the trip response curve was measured in the same manner as described in Chapter 6, i.e. a load with a known current demand was powered from the SSPC and the time duration from the SSPC turning on, to the time it tripped off, was then measured. Where the time to trip was likely to be less than 10 seconds a digital timer counter was used to record the time period. For trip times in excess of 10 seconds the measurement was performed manually with the aid of a stopwatch. Owing to limitations in the power supply, tests were performed using the 270V SSPC but powered from the 26V battery supply. In this manner the SSPC could be tested with a load current up to the required 10 PU as specified in MS3320 (i.e. 100A). In practice however only 4 PU was required owing to the SSPC current limitation circuit.

Figure 9.20 presents the recorded results of this test together with the theoretical trip response for this SSPC:

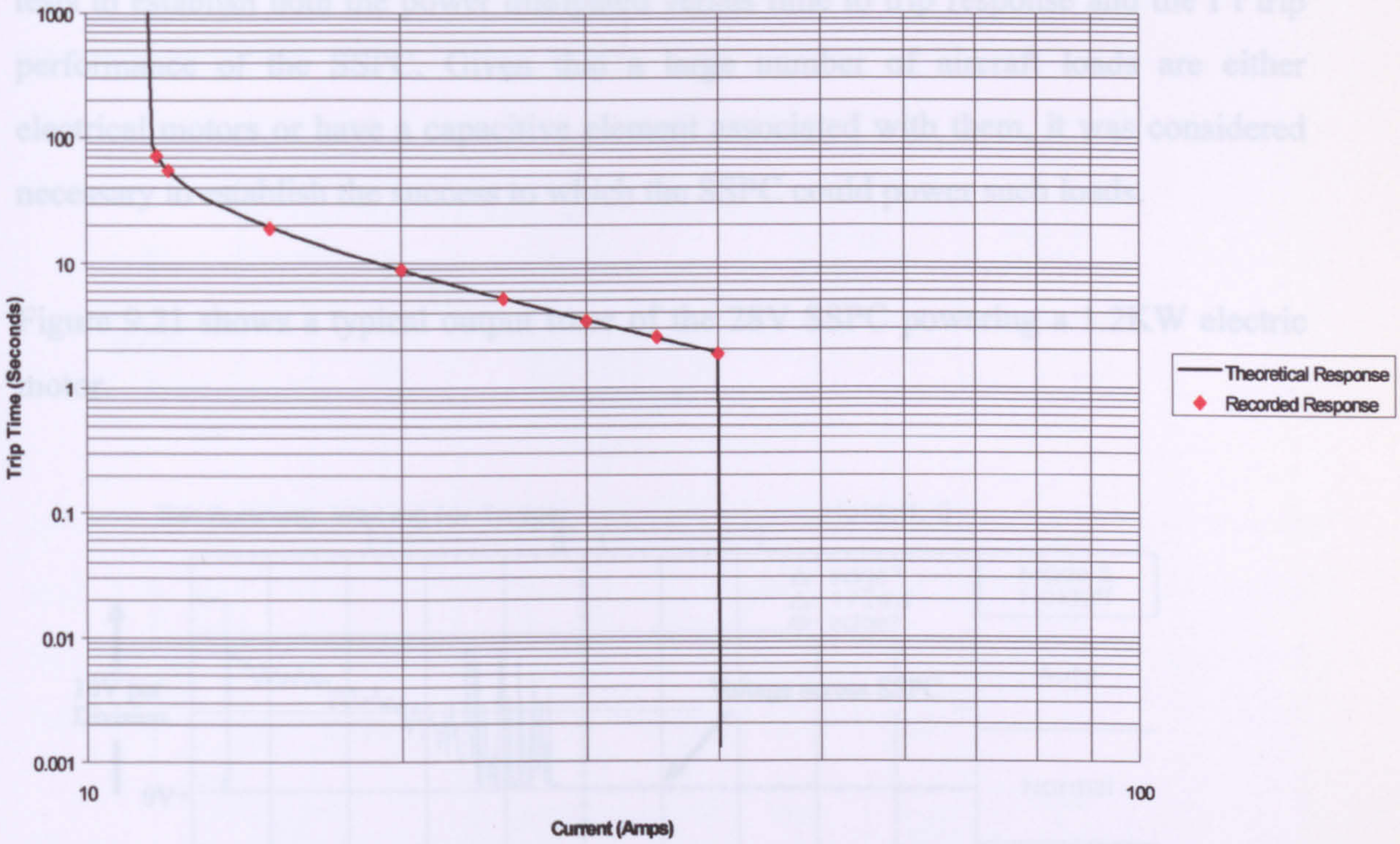


Figure 9.20 Comparison of Theoretical and Actual Trip times for I^2t

From the above chart it can observed that the recorded results agree very closely to that of the theoretical trip response. The maximum error of any of the recorded times compared to its theoretical figure was 2.11% (this figure is subject to a small amount of interpretation for trip times over, but close to 10 seconds owing the manual method used for recording time).

A notable feature of the I^2t curve in the SSPC implementation is the truncation of the trip response at 4 times the nominal load current. As mentioned previously, this feature is caused by the SSPC current limit and consequently the trip time from 2 seconds to 1.3ms is dependent on the die temperature safe operating trip response detailed in Figure 9.18.

9.7.4 Motor Load and Capacitive Load Tests

As was highlighted in Section 9.7.1, a purely resistive electrical load was used in the tests to establish both the power dissipated versus time to trip response and the I^2t trip performance of the SSPC. Given that a large number of aircraft loads are either electrical motors or have a capacitive element associated with them, it was considered necessary to establish the success to which the SSPC could power such loads.

Figure 9.21 shows a typical output trace of the 28V SSPC powering a 1.2KW electric motor.

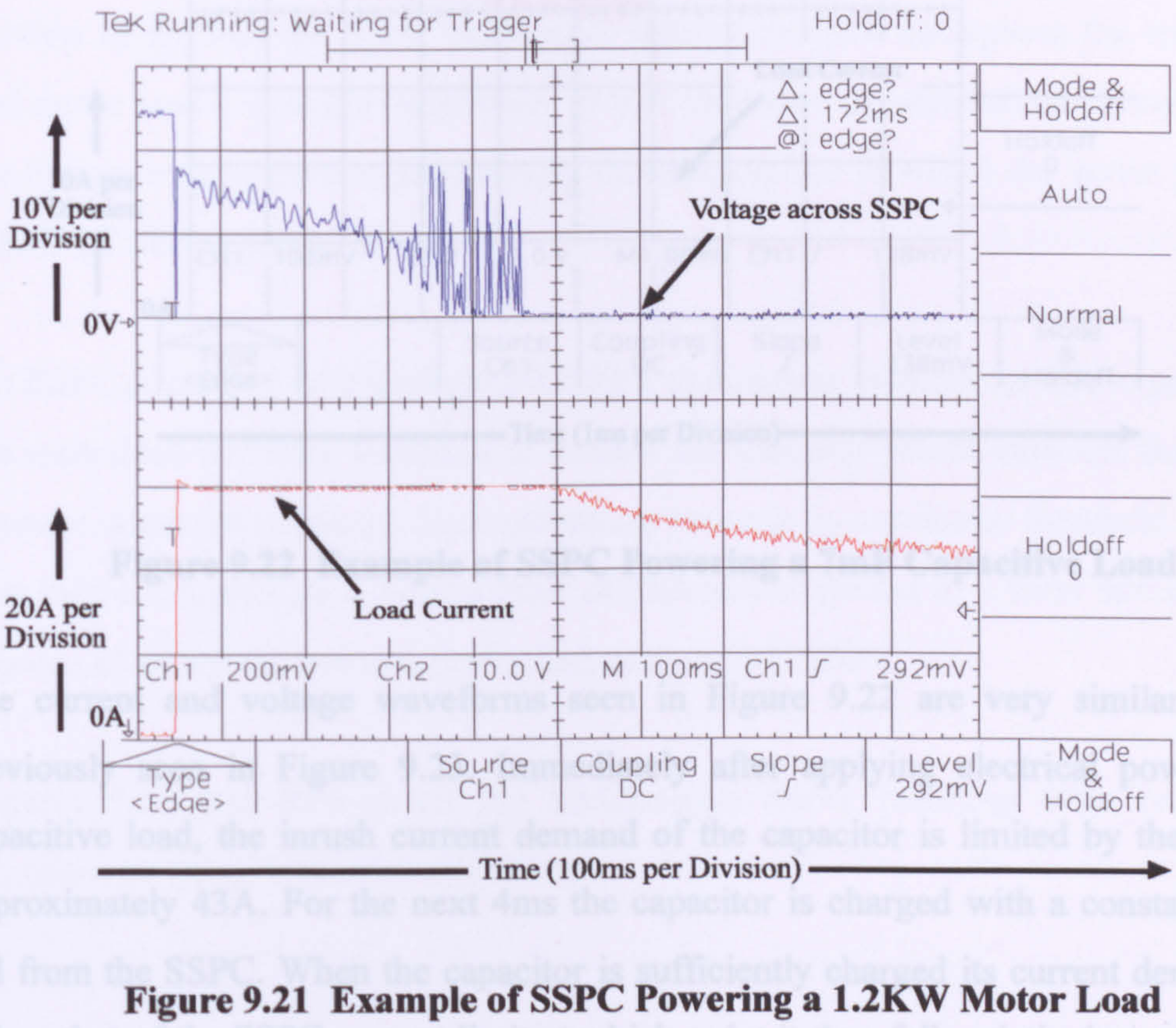


Figure 9.21 Example of SSPC Powering a 1.2KW Motor Load

From Figure 9.21 it can be observed that immediately after applying electrical power to the motor load, the SSPC limits the motor inrush current to 60A. For the next 450ms the current limit is maintained whilst the voltage across the SSPC falls steadily as the motor increases its speed of rotation. After 450ms the motor attains sufficient rotational

velocity whereby its current demand falls below that of the SSPC current limit. The motor current then gradually reduces until it eventually reaches its steady state level.

Figure 9.22 shows a trace of the SSPC powering a 10A resistive load which is connected in parallel with a 7mF capacitor.

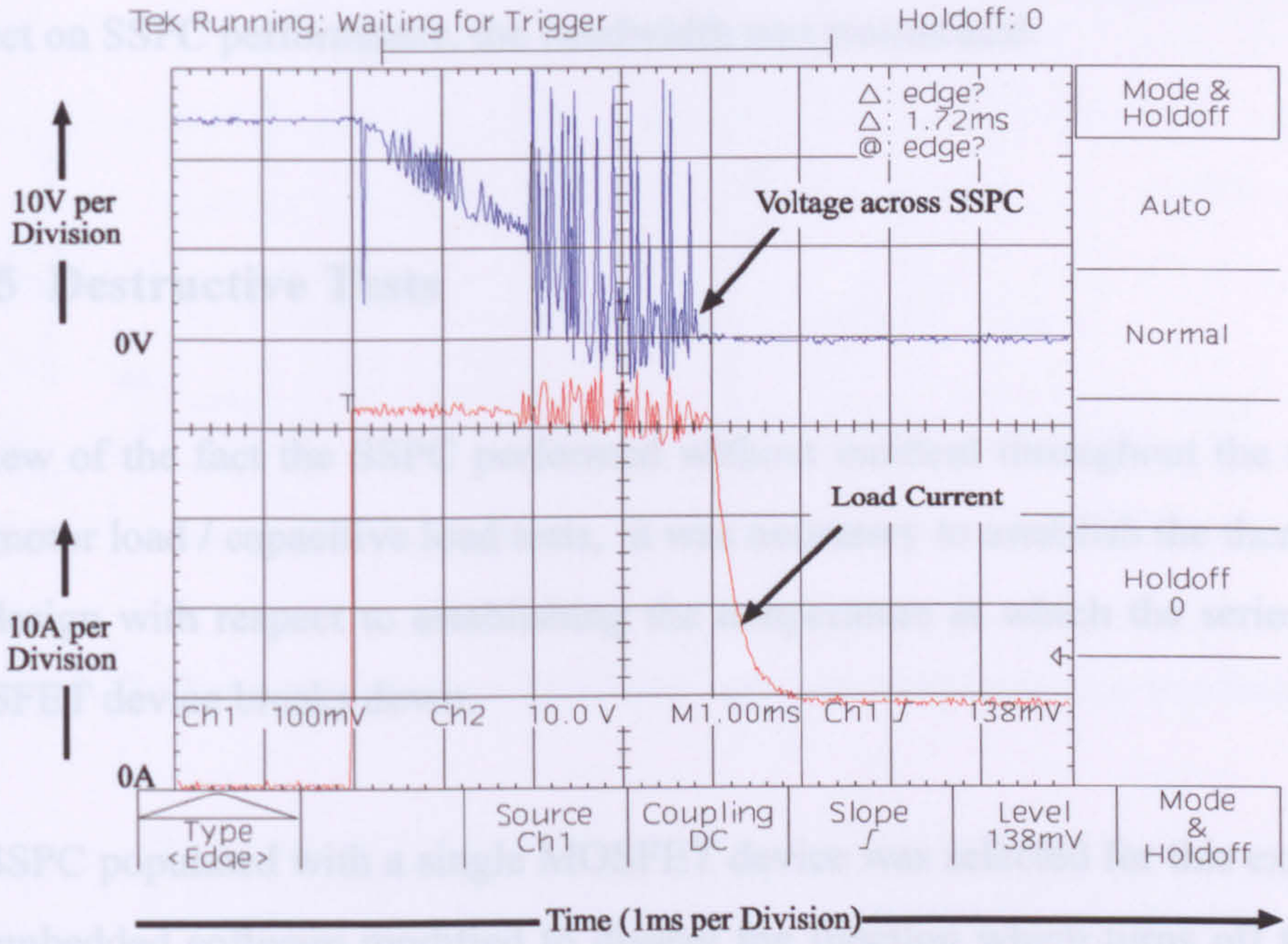


Figure 9.22 Example of SSPC Powering a 7mF Capacitive Load

The current and voltage waveforms seen in Figure 9.22 are very similar to those previously seen in Figure 9.23. Immediately after applying electrical power to the capacitive load, the inrush current demand of the capacitor is limited by the SSPC to approximately 43A. For the next 4ms the capacitor is charged with a constant current fed from the SSPC. When the capacitor is sufficiently charged its current demand falls below that of the SSPC current limit at which point it then falls relatively rapidly to the current level commanded by the load resistor.

In all the tests involving the powering on, and off of these loads, the SSPC performed without incident. From Figures 9.22 and 9.23, it can be observed that the voltage across

the SSPC displays some oscillation whilst it is performing current limitation. It was discovered that this oscillation could be minimised by reducing the bandwidth of the buffer amplifier controlling the series pass power MOSFET's. This step does however reduce the speed of response of the current limitation circuitry. Given the importance of maintaining a good response time (as was discussed in Section 9.5.3), and the fact this minor oscillation in the voltage waveform was not considered to have any significant impact on SSPC performance, the bandwidth was maintained.

9.7.5 Destructive Tests

In view of the fact the SSPC performed without incident throughout the trip accuracy and motor load / capacitive load tests, it was necessary to establish the thermal limits of the design with respect to establishing the temperature at which the series pass power MOSFET device breaks down.

An SSPC populated with a single MOSFET device was selected for this experiment and the embedded software modified to disable the function which turns off the switching element when the predicted die temperature exceeds its maximum threshold. The SSPC was then configured to a current limit of 25A and subjected to a short circuit load. For reasons of safety the test was performed using a 28V SSPC.

Figures 9.23 and 9.24 detail the oscilloscope traces resulting from two identical experiments using these test conditions.

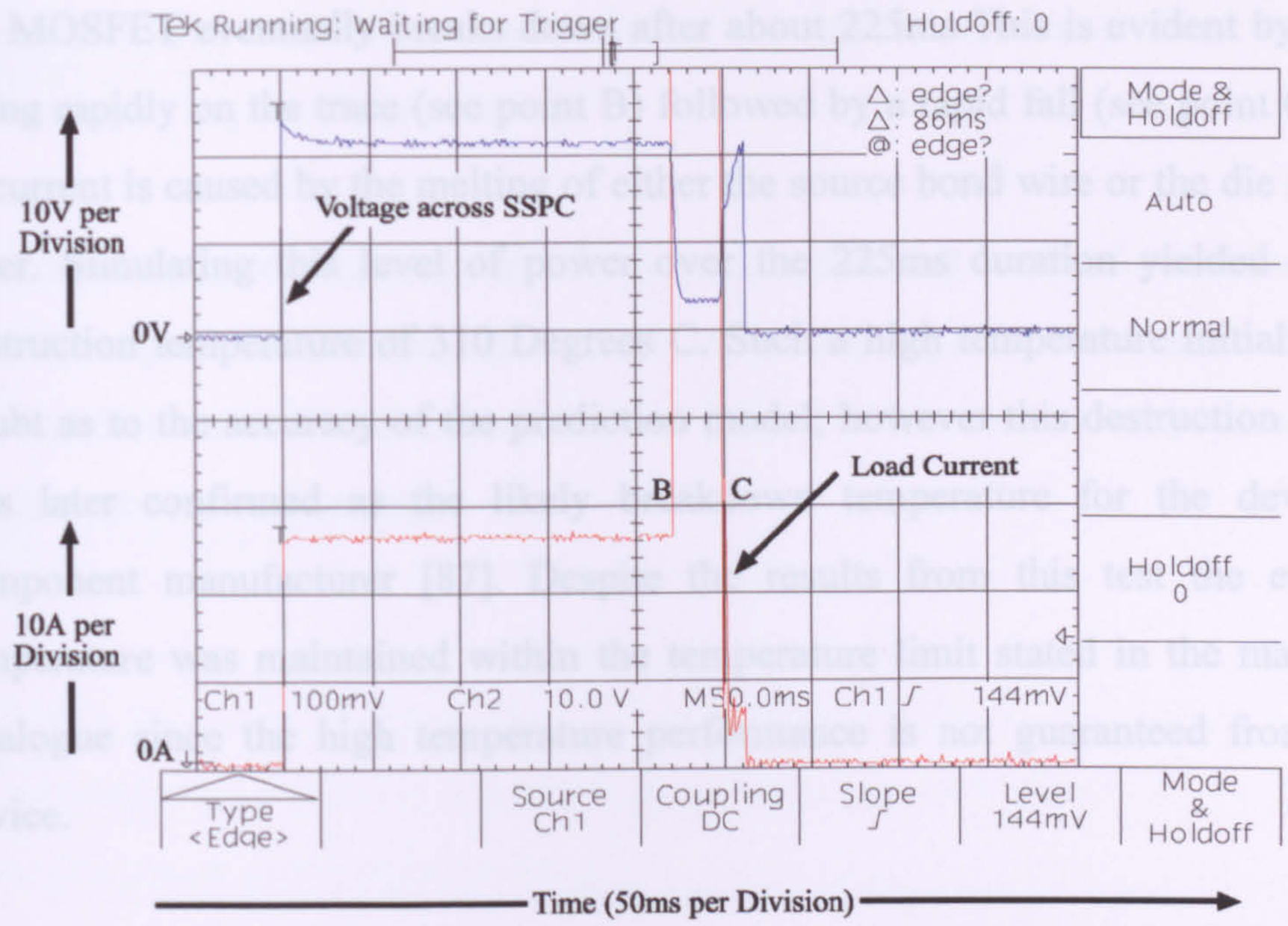


Figure 9.23 Destruction of an IRFP054 -1 when subjected to a continuous 570W

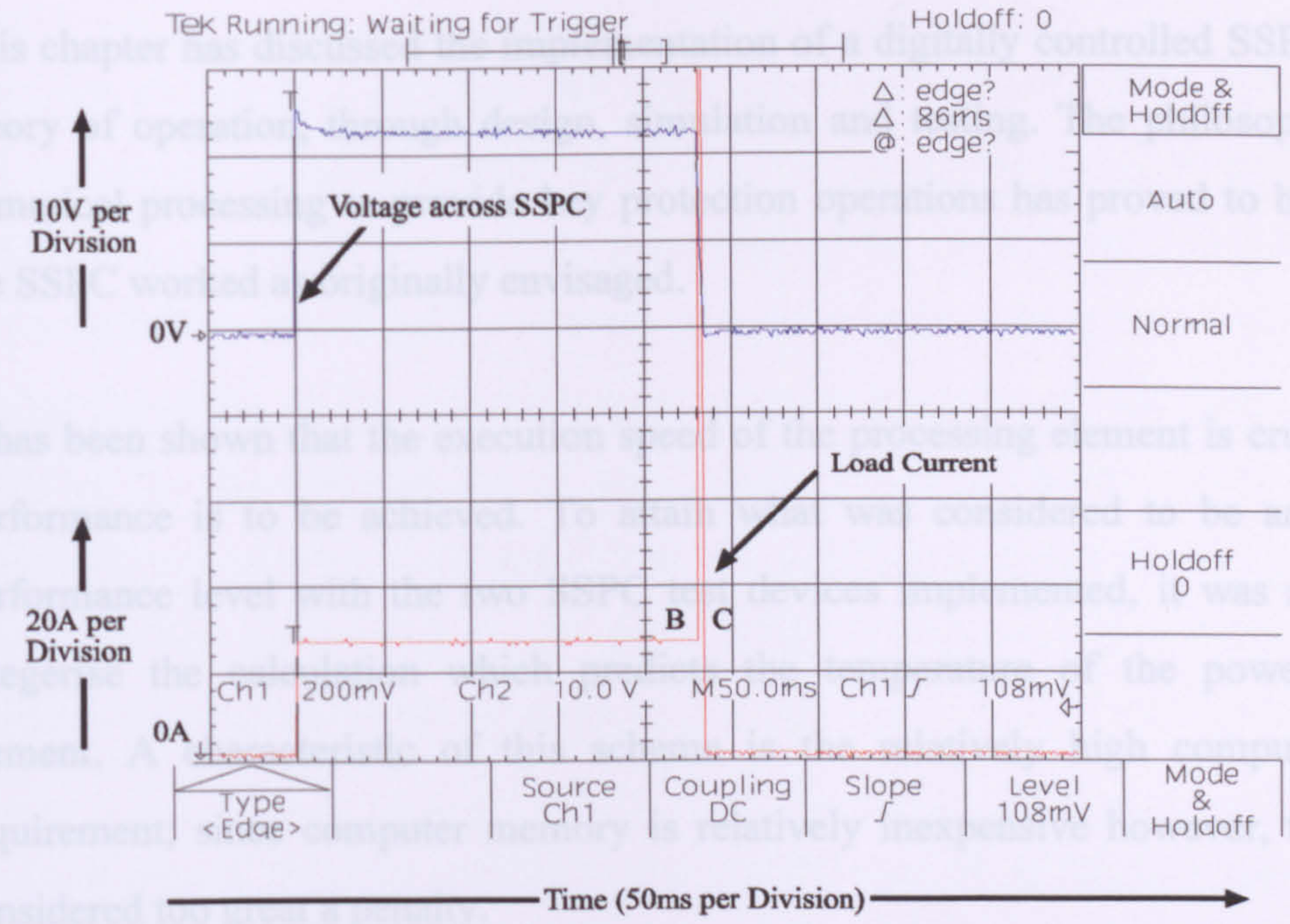


Figure 9.24 Destruction of an IRFP054 -2 when subjected to a continuous 570W

From the two example waveforms showing device destruction it can be observed that the MOSFET eventually breaks down after about 225ms This is evident by the current rising rapidly on the trace (see point B) followed by a rapid fall (see point C). This fall in current is caused by the melting of either the source bond wire or the die metalisation layer. Simulating this level of power over the 225ms duration yielded an eventual destruction temperature of 310 Degrees C. Such a high temperature initially provoked doubt as to the accuracy of the prediction model; however this destruction temperature was later confirmed as the likely breakdown temperature for the device by the component manufacturer [87]. Despite the results from this test the eventual trip temperature was maintained within the temperature limit stated in the manufacturer's catalogue since the high temperature performance is not guaranteed from device to device.

9.8 Conclusions

This chapter has discussed the implementation of a digitally controlled SSPC, from the theory of operation, through design, simulation and testing. The philosophy of using numerical processing to provide key protection operations has proved to be valid, and the SSPC worked as originally envisaged.

It has been shown that the execution speed of the processing element is crucial if good performance is to be achieved. To attain what was considered to be an acceptable performance level with the two SSPC test devices implemented, it was necessary to integerise the calculation which predicts the temperature of the power switching element. A characteristic of this scheme is the relatively high computer memory requirement; since computer memory is relatively inexpensive however, this was not considered too great a penalty.

The theory and technique of altering the SSPC current limit to follow the electrical load current demand has been discussed. This technique proved to operate successfully on

the prototype devices and is instrumental in improving the SSPC insensitivity to transient overload conditions and reducing the impact of a short circuit on the power source supplying the electrical loads.

In addition to providing protection from short circuit and overload conditions the SSPC was also capable of detecting open circuit load faults together with faults which result in a lower than normal load current demand (this is a characteristic of poor connection to the load or electrical arcing).

Chapter 10

Conclusions and Further Work

10.1 Conclusions

The aim of the this thesis was to investigate ways of improving the integrity, performance and flexibility of Solid State Power Controllers (SSPC's) for use in aircraft electrical power distribution systems.

The technique of incorporating a computing device in the form of a microcontroller into the SSPC was identified as a key way of achieving these goals.

From the viewpoint of integrity, the study has shown that an SSPC is fundamentally different from a traditional electro-mechanical device, in that its trip response is heavily dependent on the collective safe operating area of the power semiconductor used in the implementation. Under such circumstances it has been demonstrated that a software routine executing on the microcontroller provides a solution to the classic problem of ensuring the die temperature of the power switching element never exceeds its maximum temperature threshold. Likewise, a software algorithm performed on the microcontroller has been shown to create an I^2t trip response which is characteristic of older electro-thermal circuit breakers.

Ignoring current handling capability, the performance of an SSPC is measured by its insensitivity to transient overloads. Reducing nuisance tripping caused by either momentary load current surges or a load with a high inrush demand has been shown to be a function of how accurately the trip response can be calculated. A series of

measurements performed on the experimental SSPC showed the maximum deviation from a theoretical I^2t trip response to be 2.11%. This figure compares favourably with an MS3320 specification where an 80% deviation is acceptable.

It has been shown that the accuracy of the of the die temperature estimation algorithm is heavily dependent on its execution time. A fast execution time translates into a smaller tolerance that needs to be applied to the maximum trip temperature. In the experimental SSPC this tolerance was 10 Degrees C and reflects the fact the maximum power dissipation per MOSFET die was constrained to 1.35KW. If the power dissipation per die is increased beyond this limit then under the present configuration this tolerance would need to be increased owing to limitations in the processing power of the microcontroller. Despite this, the concept of predicting die temperature by performing a finite difference calculation in real time has been demonstrated to be a valid solution to ensuring the temperature never exceeds its upper limit. In addition, over the past 20 years the performance of microprocessors has consistently improved whilst the costs have continuously fallen. In the future high performance microprocessors will be sufficiently inexpensive to be used in an SSPC application. This eventuality will yield higher performance and greater accuracy since it will be possible to reduce any tolerance that needs to be applied to the die trip temperature and will facilitate the use of a more complex run time thermal model.

It has been found that one of the most tangible benefits of using numerical techniques in providing a safe operating area trip response is that the control portion of the SSPC can be easily configured for different current ratings or different semiconductor switching devices. The trip response is ultimately governed by a set of numerical parameters that can be changed at any time without requiring any hardware modifications to the SSPC control section. This is of great benefit to the manufacturer of such a device since only one controller is required regardless of the configuration of the power switching section.

Finally it has been shown that the functionality of an SSPC is increased by the integration of a computing device. The capability of comparing sampled values of load

current and switch voltage to values stored in memory which reflect normal operating levels means that faults which were previously undetectable with older elecro-thermal circuit breakers, e.g. high impedance faults and open circuit faults, can now be reported.

At a system level an integral microcontroller that can support a digital serial communications bus means that detailed information relating to SSPC status, load current, switch voltage and any other measured or calculated parameter in the SSPC can be conveyed to a controlling computer. Information of this kind can greatly assist in fault finding duties and aircraft maintenance operations. More importantly, if the central controller receives more detailed information it can make higher quality decisions regarding the configuration of the power system under crisis or abnormal conditions.

Although the particular application targeted was power distribution systems for aircraft, the results and the technology developed are equally applicable across the whole spectrum of power protection applications.

10.2 Suggestions for Further Work

This thesis has focused on the low level technology associated with switching power to an electrical load and protecting system wiring from the damaging consequences of electrical faults such as short circuits. One field of study which is a natural progression from this work is to examine the architecture of aircraft power distribution systems presently used and explore the extent to which the networked capability of the SSPC described in this thesis can be used to solve many of its problems. The following section briefly outlines these problems.

10.2.1 Problems with Existing Power Distribution Architectures

At present, it is common for the same airframe to be configured or upgraded with differing electrical equipment depending on either the operational role or the customer requirements. This situation is currently handled by the manufacturer of the airframe by creating a unique wiring loom for each electrical configuration. Such action increases the time taken to manufacture the airframe and this in turn translates to higher costs. The basic power distribution architecture as given in Figure 2.1 of Chapter 2 presents a number of obstacles when addressing the issue of efficiently handling electrical configuration changes on the same airframe.

Owing to the fact each load is connected to the load distribution centre by its own individual wire and the load distribution centre is normally some distance away from the majority of loads it is supplying, these wires are bundled together and placed within a conduit fixed to the airframe. This makes any changes or future upgrades to the content of the electrical system very expensive to implement since a significant portion of the aircraft must be dismantled in order that the wiring be removed, modified and replaced.

In a similar manner the internal connections of the load centre are hard wired for the aircraft electrical load configuration. Power destined to a load must first be routed into a circuit breaker chosen to match the characteristics of the load, then into a switch which is controlled via a microprocessor port and finally to a connector which mates with the airframe wiring. This electrical path is unique to each load in the system and it is therefore necessary to know the electrical load configuration in advance in order to construct the load distribution centre. This has the effect of making the load distribution centre unique to that particular configuration.

The operational control software embedded in the system is also unique since the I/O interface software controlling the switches will need to know at compile time which I/O ports are connected to which switches. Such a constraint makes it necessary to rework the software for each variant.

A load distribution centre has only a certain amount of spare capacity in which to accommodate any additions to the electrical system. With the present architecture the scenario where a load centre may not have sufficient spare capacity to cope with a major change is a real possibility.

Each wire connecting a load to a load centre must have a power rating equal to the maximum current demand of that load. A typical load analysis of an aircraft [88] shows that on average only 64% of the aircraft loads are energised at any one time. It is this load analysis however which is used to determine the power capability and consequently the ultimate size of the aircraft generators. The smaller the generator the greater saving in weight, size and fuel. Despite the fact savings can be made with the weight of the generators, no such saving can be made with the weight of the aircraft wiring with the present architecture since point to point wiring is not amenable to this form of power aggregation. Even if a load is only powered for 20% of the flight time the wire cannot be down sized to take advantage of this since it still must be capable of carrying the full current during the 20% on time.

10.2.2 Proposed Power Distribution Architecture

Future work directed at addressing these problems could involve the detailed examination of a aircraft power distribution architecture similar to that presented in Figure 10.1. A patent 'Power Control Connector', Patent No 9406625 has been filed to cover the concepts and details of this architecture. A copy of this patent is provided in Appendix 3.

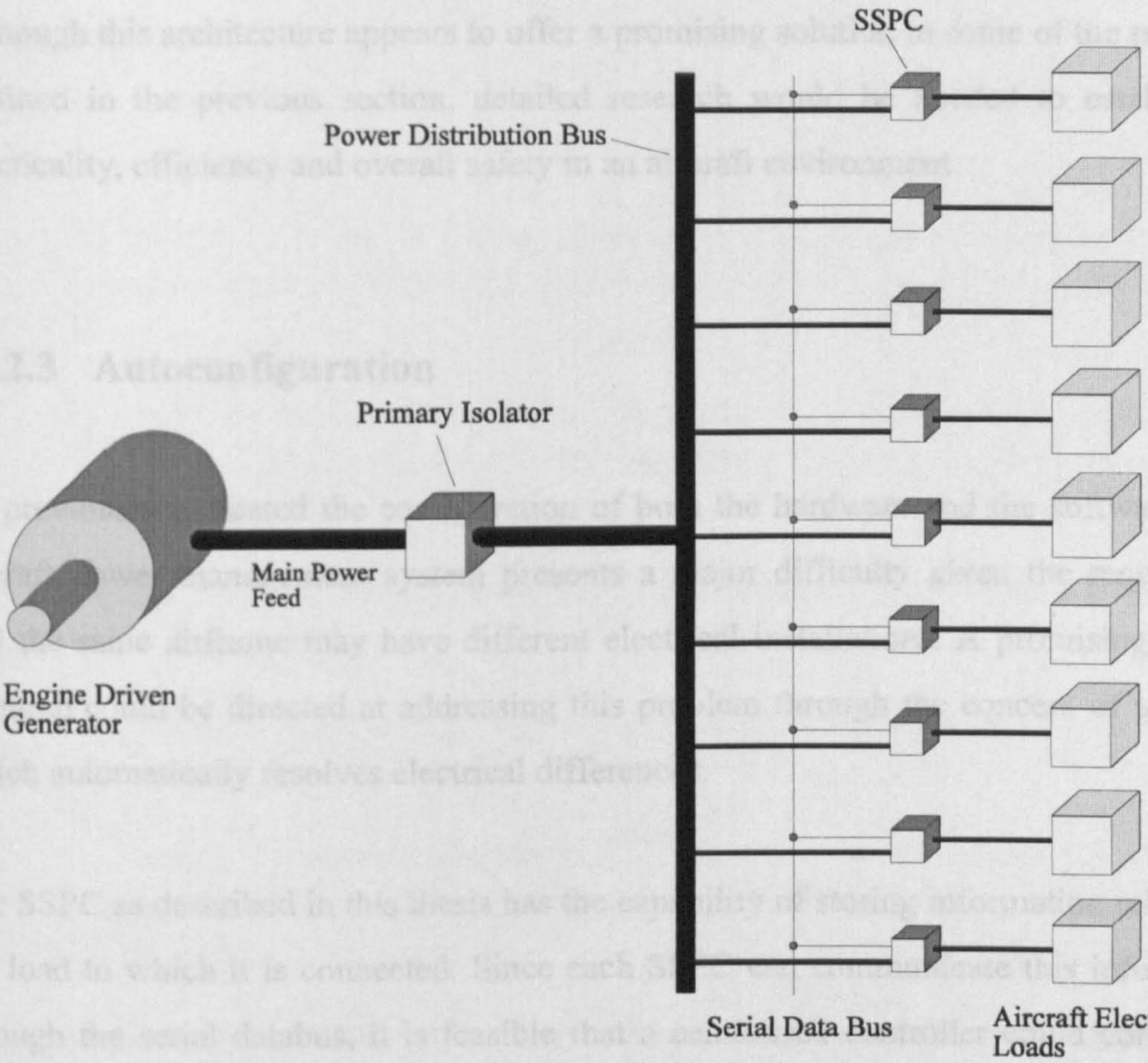


Figure 10.1 Schematic of Alternative Power Distribution Architecture

This proposed power distribution architecture dispenses with the requirement for a centralised distribution cabinet. Each aircraft electrical load instead connects to the power bus through an SSPC which is located local to the load (or built into the mating socket of the avionics connector - see Appendix 3). In the aircraft the power bus could be routed so as to always be near electronic equipment bays and other electrical items. As such, only a short spur of wire would be needed to connect the load to the power bus. This implementation thus removes the requirement for long lengths of point to point wiring and the inflexibility caused by the need for conduit bundling. If a new electronic item is to be added to the aircraft, providing there is sufficient stowage space and electrical generating capacity all it need do is connect to the power and databus via an SSPC.

Although this architecture appears to offer a promising solution to some of the problems outlined in the previous section, detailed research would be needed to establish its practicality, efficiency and overall safety in an aircraft environment.

10.2.3 Autoconfiguration

As previously indicated the configuration of both the hardware and the software in an aircraft power management system presents a major difficulty given the requirement that the same airframe may have different electrical installations. A promising area of research could be directed at addressing this problem through the concept of a system which automatically resolves electrical differences.

The SSPC as described in this thesis has the capability of storing information relating to the load to which it is connected. Since each SSPC can communicate this information through the serial databus, it is feasible that a centralised controller could construct a comprehensive database of installed loads which have reported to be present on the aircraft. In a similar manner this information could then be used in the creation of a conceptual 'operating system' through which aircraft electrical loads can be controlled. Application software from the cockpit systems which ultimately command the energisation of the electrical loads would interface with this operating system and controller functions linked through software to their respective electrical loads. Any controller without a load to control or vice versa could be flagged as a system error.

If such a scheme could be made to work there would no longer be a requirement that the aircraft electrical load configuration is hard wired into the load distribution centre since the mapping of loads to controllers would be performed logically. This scenario would then allow the manufacture of only one variant of the power distribution system regardless of the eventual electrical load content of the aircraft.

References

[1] W. Murray, L. Feiner, R. Flores. *Evaluation of All Electric Secondary Power for Transport Aircraft*. NASA Contractor Report 189077, pp. 33, 54, Appendix G1-15.

[2] D. Renz. *Comparison of All-Electric Secondary Power Systems for Civil Transport*. 27th Intersociety Energy Conversion Engineering Conference Proceedings, Vol 2, 1992.

[3] Automated Power Management, Leech International Promotional Information, Leach Corporation.

[4] I. Moir. *Load Management*. Aircraft Generation and Distribution Systems, Royal Aeronautical Society, October 1992. pp 6.1 - 6.9

[5] C. Tenning. *Evolution of the Boeing 777 Electrical Power System*. Conference Proceedings, 27th Intersociety Energy Conversion Engineering, Vol 2, 1992 pp 2.455 - 2.460.

[6] D. Kramer. *Matching Todays Technology to the Electric Power Requirement*. Aircraft Generation and Distribution Systems, Royal Aeronautical Society, October 1992. pp 2.1 - 2.10.

[7] H. Sauer. *Modern Relay Technology*. Verlag, Heidelberg, 1986.

[8] B. Bose. *Evaluation of Modern Power Semiconductor Devices and Future Trends of Converters*. IEEE Transactions on Industry Applications, Vol.28, No.2, March 1992. pp 403 - 412.

[9] *Microelectronic Relay Designers Manual*, Sixth Edition, International Rectifier Corporation 1995.

[10] A. Bishop. *Solid State Relay Handbook*. Crydom Company, 1988.

[11] X. Tian, G. Lentz. *The state of the art for solid state interruption*. EPE Journal Vol. 2, no 4, December 1992.

[12] J. Douglas. *The delivery system of the future*. EPRI Journal, Vol.17, No 7, pages 4-11, October 1992.

[13] J. De Palma, J. Rousseau and D. Ligot. *100A / 660V Static Circuit Breaker*. PCIM 93 Europe official proceedings of the 26th International Power Conversion Conference, June 1993 pages 93-102.

[14] MOS Controlled Thyristor User Guide, Harris Semiconductor 1993.

[15] B. Kovacevic. *MOSFET Pre-Driver Enhances Solid State dc Circuit Breaker.* Power Conversion and Intelligent Motion, Vol 18, 1992, pages 8 - 9, 11 - 14.

[16] A. Capel, P. Rossel, D. O'Sullivan, D. Levins and J. Ferrante. *The Electronic Solid State Switch - An Automatic Protection for Spacecraft High-Power Lines.* ESA Journal 1981, Vol.5, No.3 pages 197 - 212.

[17] J. Sturman. *Design of High Voltage High Power Solid State Remote Power Controllers for Aerospace Applications.* Proceedings 16th Annual IEEE PESC, June 1985, pp 207 - 215.

[18] S. Friedman. *Solid State Power Controller for the Next Generation.* IEEE AES Systems Magazine September 1992.

[19] X. Xiaohua, W. Tiajun and Hongmao C. *AC Solid State Power Controller* Modelling, Simulation and Control 1991, Vol 40, Issue 3 pages 41 - 45.

[20] D. Levins and F. Fachinetti. *120V 10A Solid StatePower Controller.* Proceedings of the 26th Intersociety Energy Conversion Engineering Conference, August 1991, Vol.1, pages 110 - 115.

[21] F. Fachinetti and D. Levins. *120V 10A SSPC for the Columbus Programme.* Proceedings of the European Space Power Conference, October 1989, pages 33 - 38.

[22] C. Neveu and D. Levins. Design and Development of a Current Limited Solid State Switch. Proceedings ESA Sessions at the 16th Annual IEEE PESC, June 1985, pages 281 - 285.

[23] D. Baker and G. Sundberg. *Solid State Remote Power Controllers for 120V dc Power Systems.* Proceedings, 24th Relay Conference, National Association of Relay Manufacturers, 1976, pp. 10-1 to 10-15.

[24] Solid State Power Controller with Power Switch Protection, United States Patent, Patent Number 5,444,590 August 1995.

[25] D. Grant. *Advances in Power Semiconductor Devices for Machine Control.* Proceedings International Conference on Electric Machines, September 1992, Vol.1, Pages 22 - 28.

[26] Semilab Shortform Catalog 1995, Semilab PLC.

[27] Power Semiconductor Product Digest Short Form Catalog, International Rectifier Corporation 1994.

[28] Mitsubusi Semiconductors General Catalogue 1995, Mitsubusi Electric Corporation.

[29] S. Clemente, A. Dubhashi, B. Pelly. *IGBT Characteristics.* Application Paper AN-983A, International Rectifier Corporation 1994.

[30] IGBT Module and Discrete Device Catalogue, Hitachi 1995.

[31] US Department of Defense MIL-STD-704D, Aircraft Electrical Power Characteristic, September 1980.

[32] Survey of Aircraft Loads for the B777-200, Boeing Aircraft Corporation, Extract from Analysis Document LS-CC-32359, April 1995.

[33] Development Specification for C-130J ECBU, J12K03-102, Lockheed Martin Corporation, June 1993.

[34] IGBT Designers Manual, International Rectifier Corporation 1994.

[35] HEXFET Power MOSFET Designers Manual, Vol.3, September 1993, International Rectifier.

[36] R. Letor. *Static and Dynamic Behavour of Paralleled IGBT's.* IEEE Transactions on Industry Applications, Vol.28, No.2, March 1992.

[37] D. Dapkus. *Parallel Operation of IGBT's.* Application Paper DT-946, International Rectifier Corporation 1994.

[38] H. Vogt. *Smart Power Technology with Dielectric Insulation Processes and Applications.* Electron Technology 26, Institute of Electron Technology, Warszawa 1993, pages 83 - 93.

[39] T. Ohno, M. Satoshi and I. Katsutoshi I. *An Intelligent Power IC with Double Buried-Oxide Layers Formed by SIMOX Technology.* IEEE Transactions on Electron Devices, Vol 40, No.11, November 1993.

[40] Automotive Products Databook, 2nd Edition, SGS-Thompson Microelectronics, January 1993.

[41] D. Navon. *Electronic Materials and Devices.* Houghton Mifflin Company 1975.

[42] Mospower Applications Handbook - Siliconix Incorporated 1985

[43] D. Paul and S. Venugopalan. *Power Distribution System Equipment Overvoltage Protection.* IEEE Industrial Applications Meeting, Vol. 2, 1993.

[45] C. Neugebauer, A.Yerman, R. Carlson, J. Burgess, H. Webster and H. Glascock. *The packaging of power semiconductor devices*. Gordon and Breach Science publishers ISSN 0275-7230.

[46] H. Yilmaz, T. Tsui, I. Bencuya, T. Fortier and K. Owyang. *Safe Operating Area of Power DMOS FET's.* PESC 89 Record. 20th Annual IEEE Power Electronics Specialists Conference, 1989, Vol. 1, pages170-175.

[47] G. Meyer. *On the theory of fuses*. Munich 1906.

[48] IEEE committee report. *Computer representation of overcurrent relay characteristics*. Transactions on Power Delivery, Vol. 4, No. 3, July 1989, pages. 1659 - 1667.

[49] MS3320 Time Current Characteristic Specification Keuffel & Esser Co. Oct 1989.

[50] J. Fidinger and J. Vincent. *Low voltage circuit breaker modernisation through solid state technology*. Industrial Applications Society 38th annual Petrolium and Chemical Industry Conference, 1991, pages 193 - 197.

[51] J. Urie. *Specifying a circuit breaker for your product*. Electrical Manufacturing, May/June 1992 pages. 18-19

[52] K. Balasubramanian. *Eprom based overcurrent relays*. Proceedings of the 38th IEEE Holm Conference on Electrical Contacts 1992, pages 203-207.

[53] British Standards BS142 Electrical Protection Relays Part 1 Section 1.1 and 1.2, 1982

[54] I. Purkayastha and P. Savoie. *RMS digital trips offer increased accuracy and reliability advances in low voltage circuit breaker trip technology*. IEEE Transactions on Industrial Applications, 1990, Vol 26. No. 1, pages 160-166.

[55] S. Chowdhury, T. Chowdhury and S. Banerjee. *Software implementation of overcurrent relay characteristics for industrial power systems protection.* Modelling Measurements and control, A,AMSE Press Vol 53, No 4, 1993, pages 41 - 44.

[56] J. Holman. *Heat Transfer*. McGraw-Hill Kogakusha, Fifth Edition, 1981

[57] S. Clemente. *Transient thermal response of power semiconductors to short power pulses*. IEEE Transactions on Power Electronics, Vol 8, issue 4, Pages 337 - 341, Oct 1993.

[58] F. Oettinger, D. Blackburn and S. Rubin. *Thermal Characterisation of Power Transistors*. IEEE Transactions on Electron Devices, Vol. ED-23, Aug 1976 pages 831-838.

[59] D. Blackburn and D. Berning. *Power MOSFET Temperature Measurements*, PESC 82 Record pages. 400-407.

[60] Z. Jakopovic. *Computer Controlled Measurement of Power MOSFET Transient Thermal Response*. 23rd Annual IEEE Power Electronics Specialist Conference, July 1992, Vol. 2, pages 1026-1032.

[61] R. Severns. *Safe Operating Area and Thermal Design for MOSPower Transistors*. MOSPOWER Applications Handbook Siliconix Incorporated 1985.

[62] P. Gray, D. DeWitt, A. Boothroyd and J. Gibbons. *Physical Electronics and Circuit Models of Transistors*. SEEC Series, Volume 2 (John Wiley and Sons, New York, 1964), pages 47-50.

[63] J. Fergason. *Liquid Crystals in Nondestructive Testing*. Applied Optics, Vol.7, No.9, Sept 1968, pages 1729-1737.

[64] C. Stephens and S. Sinnadurai. *A surface temperature limit detector using nematic liquid crystals with an application to microcircuits*. Journal of Physics E: Scientific Instruments, Vol.7, 1974, pages 641-643.

[65] H. Macksey, R. Adams, D. McQuiddy, D. Shaw and W. Wisseman. *Dependance of GaAs Power MESFET Microwave Performance on Device and Material Parameter*. IEEE Transactions on Electronic Devices, Vol 2, ED-33 No 10, October 1986.

[66] Private communication between K.P. Thomas and Dr P.W.Webb.

[67] D. Griffin. *Infrared Techniques for Measuring Temperature and Related Phenomena of Microcircuits*. Applied Optica, Vol.7, No.9, Sept.1968, pages 1749-1756.

[68] P. Webb. *Measurement of Thermal Transients in Semiconductor Power Devices and Circuits*. IEEE Proceedings, Vol.130, Pt.1, No.4, Aug.1983.

[69] X. Tian. and R. Moussanet. *Current Measurement using Switch Voltage Drop in IGBT dc Circuit Breaker Application*. IEE, Fifth European Conference on Power Electronics and Applications, Sept 1993, pages 332-336

[70] H. Carslaw and J. Jaeger. *Conduction of Heat in Solids*. Second Edition Oxford University Press 1959.

[71] P. Schneider. *Conduction Heat Transfer*. Addison-Wesley, Reading, Mass 1955.

[72] V. Arpaci. *Conduction Heat Transfer*. Addison-Wesley, Reading, Mass 1966.

[73] P. Webb and G. Xiang. *Implementation of Timestep Changes in Transmission Line Matrix Diffusion Modelling*. International Journal of Numerical Modelling, Vol.5, pages 251-257 1992.

[74] Phoenics 1.4, Concentration, Heat and Momentum Limited

[75] Electronics Weekly. *New MOSFET Family gives low on resistance*. April 26th 1995.

[76] E. Schmidt. *On the application of the Calculus of Finite Differences to Technical Heating and Cooling Problems*. Julius Springer, Berlin, 1924, pages 179 - 184.

[77] G. Myers. *Analogue Methods in Conduction Heat Transfer*. McGraw-Hill, New York, 1971.

[78] M. Ozisik. *Boundary Value Problems of Heat Conduction*. International Textbook Company, Scranton, Pa. 1968.

[79] W. Newell. *Transient Thermal Analysis of Solid-State Power Devices-Making a Dreaded Process Easy*. IEEE Transactions on Industry Applications, Vol. 1A-12, No.4, July/August 1976.

[80] P. Hammond. *Engineering Electromagnetism Physical Processes and Computation*. Oxford University Press 1994.

[81] S. Sueker. *Transient Thermal Impedance Modelling of Semiconductor Heat Sinking*. IEEE Industrial Applications Conference, 28th Annual Conference Proceedings, Vol 2, Oct 1993, pages. 1238 - 1241.

[82] D. Dean. *Thermal Design of Electronic Circuit Boards and Packages*. Electrochemical Publications 1985. 8 Barns Street Ayr Scotland.

[83] P. Maycock. *Thermal Conductivity of Silicon Germanium, III-V Compounds and III-V Alloys*. Solid State Electronics, Pergamon Press 1967. Vol. 10, pages 161-168.

[84] Private conversation between K.P. Thomas and J. Davey Smiths Industries Defense Systems North America

[85] Siemens C167CR CAN Version User Manual Version 0.0 Advanced Information 7.94, Siemens AG July 1994.

[86] K. Gauen. *Parralleling Power MOSFETs in Linear Applications.* Proceedings of PCI 1994, April 1984, Atlantic City, pages 144 - 151.

[87] Private conversation between K.P Thomas and Mr Woodford of International Rectifier Oxted Surrey.

[88] Canadair Global Express Electrical Load Management System. Volume 1 Technical CTSP 3994, March 1993.

Bibliography

Arpaci. V. *Conduction Heat Transfer*. Addison-Wesley, Reading, Mass 1966.

Bishop. A. *Solid State Relay Handbook*. Crydom Company, 1988.

Carslaw. H and Jaeger. J. *Conduction of Heat in Solids*. Second Edition Oxford University Press 1959.

Dean. D. *Thermal Design of Electronic Circuit Boards and Packages*. Electro-chemical Publications 1985. 8 Barns Street Ayr Scotland.

Hammond. P. *Engineering Electromagnetism Physical Processes and Computation*. Oxford University Press 1994.

Hitachi IGBT. Module and Discrete Device Catalogue 1995.

Holman. J. *Heat Transfer*. McGraw-Hill Kogakusha, Fifth Edition, 1981.

International Rectifier Corporation. HEXFET Power MOSFET Designers Manual, Vol.3, September 1993.

International Rectifier Corporation. IGBT Designers Manual 1994.

International Rectifier Corporation. Microelectronic Relay Designers Manual, Sixth Edition, 1995.

International Rectifier Corporation. Power Semiconductor Product Digest Short Form Catalog 1994.

Mitsubusi Electric Corporation. Mitsubusi Semiconductors General Catalogue 1995.

Myers. G. *Analogue Methods in Conduction Heat Transfer*. McGraw-Hill, New York, 1971.

Neugebauer. C, Yerman. A, Carlson. R, Burgess. J, Webster. H, and Glascock. H. *The packaging of power semiconductor devices*. Gordon and Breach Science publishers ISSN 0275-7230.

Ozisik. M. *Boundary Value Problems of Heat Conduction*. International Textbook Company, Scranton, Pa. 1968.

Sauer. H. *Modern Relay Technology*. Verlag, Heidelberg, 1986.

Schneider. P. *Conduction Heat Transfer*. Addison-Wesley, Reading, Mass 1955.

Semilab PLC. Semilab Shortform Catalog 1995.

SGS-Thompson Microelectronics. Automotive Products Databook, 2nd Edition, January 1993.

Siemens AG. C167CR CAN Version User Manual Version 0.0 Advanced Information 7.94, July 1994.

Siliconix Incorporated. Mospower Applications Handbook 1985.

Glossary and Abbreviations

Relay	An electrical switch which can be controlled remotely by virtue of an electrical signal.
Circuit Breaker	An electrical device used to provide protection from excessively high circuit currents.
SSPC	Solid State Power Controller. A device which uses power semiconductors to provide the actions of an electrical relay switch and a fuse or circuit breaker.
MOSFET	Metal Oxide Silicon Field Effect Transistor. A three terminal semiconductor switch where the magnitude of electrical current flow between two of the terminals is under the continuous control of the voltage on the third.
IGBT	Insulated Gate Bipolar Transistor. A three terminal semiconductor switch where the magnitude of electrical current flow between two of the terminals is under the continuous control of the voltage on the third.
BJT	Bipolar Junction Transistor. A three terminal semiconductor switch where the magnitude of electrical current flow between two of the terminals is under the continuous control of the current into the third.

MCT	Mos Controlled Thyristor. A three terminal semiconductor switch where the electrical current flow between two of the terminals is under the control of the voltage on the third.
GTO	Gate Turn Off Thyristor. A three terminal semiconductor switch where the electrical current flow between two of the terminals is under the control of the voltage on the third.
SmartFet	A generic name of a type of MOSFET which has integral current overload protection circuitry.
A to D	Analogue to Digital Converter. A device which converts the amplitude of an analogue signal into a representative digital number.
PWM	Pulse Width Modulation. A digital frequency waveform where the ratio of the time the waveform is at the logical 'one' level to the time the waveform is at the logical 'zero' level is variable.
Microcontroller	A digital processor which incorporates a number of hardware peripherals i.e. timers, A to D converters, PWM units etc.
Inrush Current	The higher than normal current demand of an electrical load for a short time after power has been applied to it.
Nuisance Trip	A condition whereby a circuit breaker disconnects a circuit from the power supply when there is in actuality no electrical fault.

Appendix 1:

Patent Application for Digital Circuit Breaker

SMITHS INDUSTRIES

Aerospace • Medical Systems • Industrial

Internal Memorandum

From: **G.J. Kodish**
Location: **HQ**
Internal Tel No: **8241**
Facsimile No. **0181 201 8041**
Date: **26 July 1995**

To: **R. Fitzpatrick - CH15**
cc: **K.P. Thomas- CH15**
K.C. Rawlings - CH15

ELECTRICAL APPARATUS
9514528

The Patent Application for your DIGITAL CIRCUIT BREAKER was filed at the Patent Office on 15 July 1995 and given Application No. 9514528

A copy of the specification as filed is enclosed.

Gillian J. Kodish

ELECTRICAL APPARATUS

This invention relates to electrical apparatus and methods for controlling switching of circuit protection devices.

The usual way of protecting electrical equipment and its wiring from current overloads is by means of an electromagnetic relay switch, thermal wire fuse or an electrothermal circuit breaker. An electrothermal circuit breaker uses the current flowing through it to heat a thermal sensor. Typically this consists of a bimetallic strip thermostat heated by a resistive element which passes the current flowing through the breaker. The thermostat will operate when its temperature is raised beyond a pre-set value with the consequence that the circuit breaker will open, removing power from the load. The temperature of the thermostat at any one time is a function of the dynamic equilibrium between the heat gain from the resistive element and the heat loss to the surroundings. The resistive element will gain heat at the rate I^2R, where I is the current flowing through the resistive element and R is its resistance.

These previous arrangements, however, are usually relatively heavy and bulky. They also have a slow response time and can be unreliable in the long term. Because of this, there is a move towards using solid state power controllers (SSPC) employing power semiconductors, to switch electrical energy to a load and to interrupt current flow should an overload be detected.

Conventional electromagnetic devices, however, have an advantage not enjoyed by SSPCs in that they have an I^2t characteristic. That is, the product of the square of current I and the time to reach a critical energy level is a constant so that the time taken to trip out is inversely proportional to the square of the current. This means that the device will trip quickly for high currents but, for low currents, the trip time will be longer. Thus, a moderate excess current may not produce a trip if the current reduces after a short time. This reduces the occurrence of nuisance trips. Also, thermal protection devices have a memory in that a previous

non-trip overload will raise the temperature of the device so that, if a second overload current should occur shortly after, it would raise the temperature of the device to its trip level more quickly. This is a useful feature because the equipment and wiring protected by the device would respond in a similar way.

It has been proposed in GB 2271895 to control operation of an SSPC using a control circuit that emulates an I^2t characteristic using a network of resistors and capacitors.

Various other circuits breakers are described in GB 2140633, GB 899354, GB 1527962, GB 1524826, GB 2135146, GB 1124492, EP 5324, EP 326334 and US 4,266,259.

It is an object of the present invention to provide improved apparatus for use in power switching and an improved method of controlling switching of a circuit protection device.

According to one aspect of the present invention there is provided electrical apparatus for controlling the switching of a circuit protection device, the apparatus including means for multiplying a measurement of the current through the circuit protection device by itself to derive a voltage signal representative of current squared, means for supplying said signal to a resistor capacitor circuit having a time constant that emulates the thermal sensor of an electrothermal circuit breaker, and means supplying an output derived from said resistor capacitor circuit to control switching of the circuit protection device.

According to another aspect of the present invention there is provided electrical apparatus for controlling switching of a circuit protection device, the apparatus including a processor arranged to receive a signal representative of current through a circuit protection device, the processor calculating the resultant heat gain of an emulated thermal sensor during a short period of time, the processor calculating the resultant heat loss of the emulated thermal sensor during the said period, the processor calculating the resultant temperature of the sensor

at the end of the said period, and the processor switching the circuit protection device if the temperature exceeds a predetermined limit.

According to yet another aspect of the present invention there is provided a method of controlling switching of a circuit protection device comprising the steps of deriving a signal representative of heating of an emulated thermal sensor, deriving a signal representative of cooling of said sensor, determining the temperature of the sensor from the sum of its previous temperature and the differences between sensor heating and cooling, comparing the sensor temperature with a maximum permitted temperature, and signalling the circuit protection device to open if the maximum permitted temperature is exceeded.

An electrical system including a circuit protection device and various apparatus and methods for controlling operation of the device, in accordance with the present invention, will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of the system;

Figure 2 is a schematic diagram of an alternative system; and

Figure 3 is a graph illustrating the performance of an electromagnetic circuit breaker.

With reference to Figure 1, there is shown an electrical system including an electrical circuit comprising electrical equipment 1 and associated wiring 10 connected to a power source 2 via a solid state power switch 3. A current sensing device 4 supplies a signal proportional to the current flowing through the power switch 3 to both inputs of a multiplier 5. The voltage output of the multiplier 5 is connected via a resistor 6 to a first plate of a capacitor 7, which has its second plate connected to a ground reference. The first plate of the capacitor 7 is also

connected to one input of a comparator 8, the other input of which is connected to a source 9 of reference voltage. The output of the comparator 8 is connected via line 11 to the control input of the power controller 3.

The time constant of the RC network formed by the resistor 6 and capacitor 7 is selected to be the same as the desired thermal time constant of the thermal sensor of the equivalent electrothermal circuit breaker. The voltage V_c across the capacitor 7 represents the actual temperature of the emulated thermal sensor in the circuit. This is compared with the reference voltage provided by the source 9 representing the maximum temperature the emulated thermal sensor is allowed to reach.

In normal operation, the current flowing through the equipment 1 and its associated wiring 10 is below the maximum continuous current rating, so the voltage V_c across the capacitor 7 does not exceed the reference voltage and no trip will occur.

When overload conditions occur, the voltage V_c across the capacitor 7 increases until its voltage is greater than that of the reference voltage. The comparator 8 generates an output control signal to the power switch 3, causing it to open and interrupt power supply to the equipment 1 and its associated wiring 10. The time interval between the occurrence of the overload and the generation of the trip command is, therefore, dependent on the magnitude of the overload.

The ability of the capacitor to store charge gives the apparatus the equivalent of the thermal memory of a conventional thermal device. For example, if the circuit were subject to a current overload close to, but below, the trip limit for a period time, the capacitor 7 would be charged to a voltage level close to the reference voltage. When the overload is removed, the output of the multiplier 5 falls below the voltage of the capacitor, causing the capacitor to discharge through the resistor 6. This models the heating and cooling that takes place in the thermal sensor of a conventional electrothermal device. If a second overload occurred before

the capacitor had discharged significantly, the charge time to reach the critical trip threshold would be shorter. This replicates the performance of the thermal sensor of a conventional thermal device, which would not have had time to cool fully before the second overload.

In an alternative arrangement, digital techniques could be used to make calculations to emulate the performance of a conventional electrothermal circuit breaker. The exact form of heat loss to the surroundings of a conventional electrothermal device is a complex function but good agreement with I^2t curves from conventional circuit breakers has been obtained by assuming heat loss is directly proportional to the temperature difference between the thermal sensor and its surroundings. The emulation consists of a repetitive calculation of the heat loss and gain calculations, followed by comparison of the resultant temperature with a pre-set maximum. The repetition time is chosen to be sufficiently short to ensure that the power switch is actuated in a timely manner in the event of current overload and to ensure that the temperature rise during that time is sufficiently small that errors caused by assuming it to be constant are negligible.

With reference to Figure 2, the components 5 to 9 of the previous arrangement are replaced by a processor 20 having its input connected to the current sensor 4 via an analogue-to-digital converter 21.

The processor 20 contains an accumulator 22 whose value emulates the temperature of the thermal sensor in the conventional electrothermal circuit breaker, relative to ambient. When the circuit is first powered, this accumulator is pre-set to an appropriate value. In many cases the appropriate value can be zero as the load and its wiring will all be at ambient temperature.

The output of the current sensing device 4 is converted to a convenient digital form by means of the analogue-to-digital converter 21 at an appropriate regular sampling rate. Each output sample of the analogue-to-digital converter 21 is used as a new data input to the processor 20, which carries out the following steps in turn for each new data value:

(1) Calculate the gross heat gain during the sampling repeat time to the emulated thermal sensor as a function of the data value from the analogue-to-digital converter 21. Then calculate a function consisting of the product of the data input value multiplied by itself ~~and~~ or if necessary an appropriate scaling factor. It may be convenient to use a look-up table to perform this calculation. This function is required to emulate a conventional circuit breaker but alternate functions can provide modified performance if required.

(2) Add the result of (1) into the accumulator 22 whose value represents the temperature of the emulated thermal sensor.

(3) Calculate the gross heat loss from the emulated thermal sensor, as a function of the value in the accumulator. A simple linear proportionality function has been found to emulate conventional circuit breaker characteristics but alternate functions may provide modified performance if desired. A look-up table may be used to perform this calculation.

(4) Subtract the result of (3) from the contents of the accumulator 22.

(5) Compare the resultant accumulator value with a maximum emulated threshold temperature.

(6) Generate a trip command if the accumulator value exceeds the threshold.

The processor 20 could be a microprocessor or microcontroller. Alternatively, the processor could be implemented by dedicated or programmed logic devices connected in a circuit.

Instead of performing the steps set out above, the processor 20 could perform the following steps for each new data value from the A/D converter 21:

(1) The data input value is multiplied by itself to produce a value representing the square of the input value. A look-up table may be used to perform this calculation. This squared input value is then compared with the value stored in the accumulator.

(2) The following calculation is now performed :

Accumulator = squared input value - (squared input value - Accumulator).C where C represents a constant.

(3) Compare the resultant accumulator value with a maximum emulated threshold temperature.

(4) Generate a trip command if the accumulator value exceeds the threshold.

These techniques can generate a current input versus time-to-trip function similar to conventional electromagnetic circuit breakers with an I^2t performance.

Although the above techniques can function satisfactorily, because they operate iteratively, the accuracy and continuous nature of its operation is dependent on the program execution time. Depending upon circumstances, it may be necessary to implement an additional control mechanism to the power supply switch to limit damage in the event of very high current flow.

Similarly, depending upon circumstances, it may be desirable to input information from other sensors or information sources via a suitable interface, which the processor will consider to modify its control to the power switching device. An example of this would be a temperature sensor, which could be used to modify the amount of power supplied to the load in the event that the temperature exceeded pre-set limits. An alternate example would be information from another controller.

It may also be desirable for the processor to be provided with a suitable interface to communicate information known to it, for example present current flow, to external systems for more comprehensive system control.

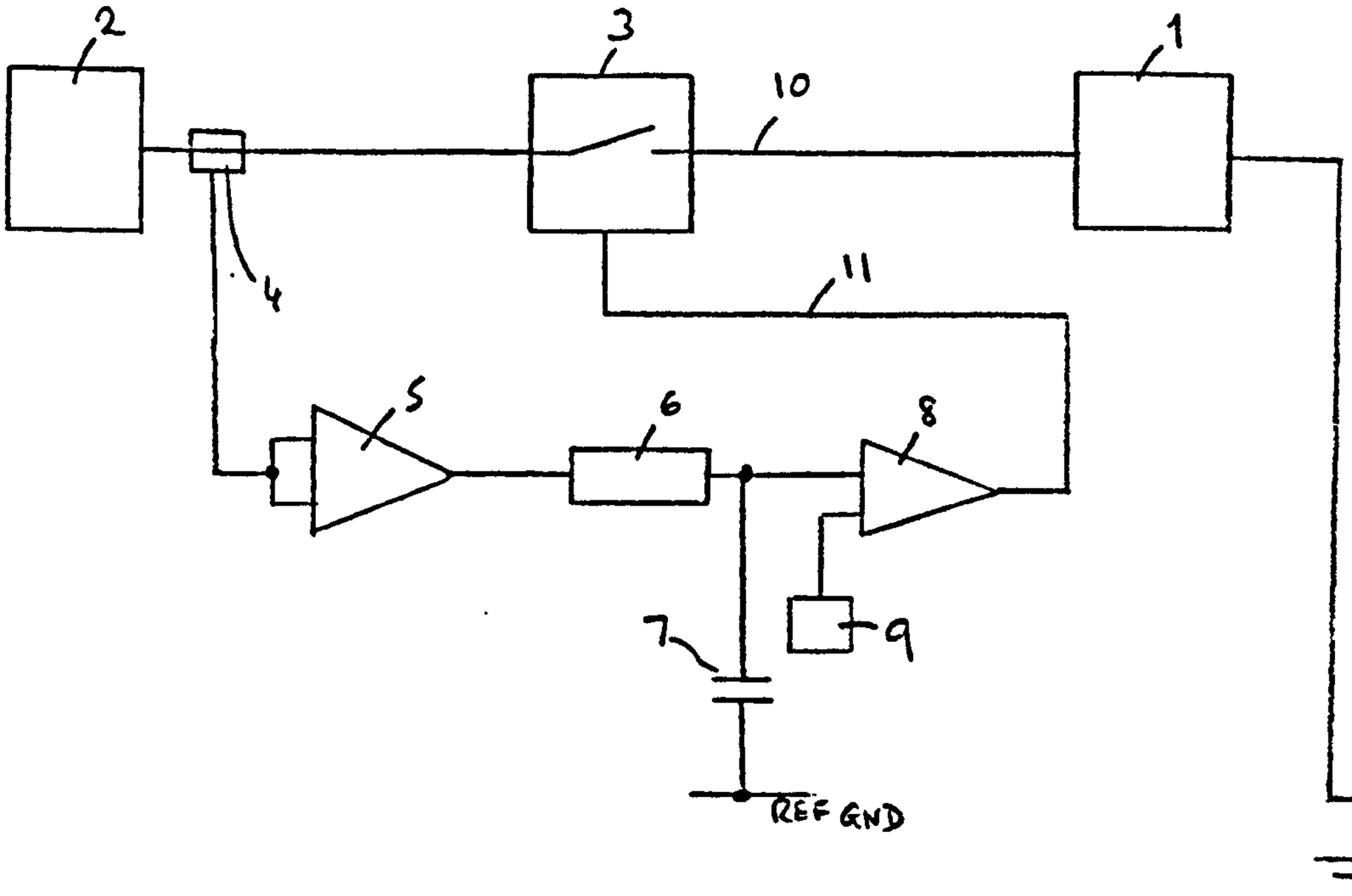


FIG. 1

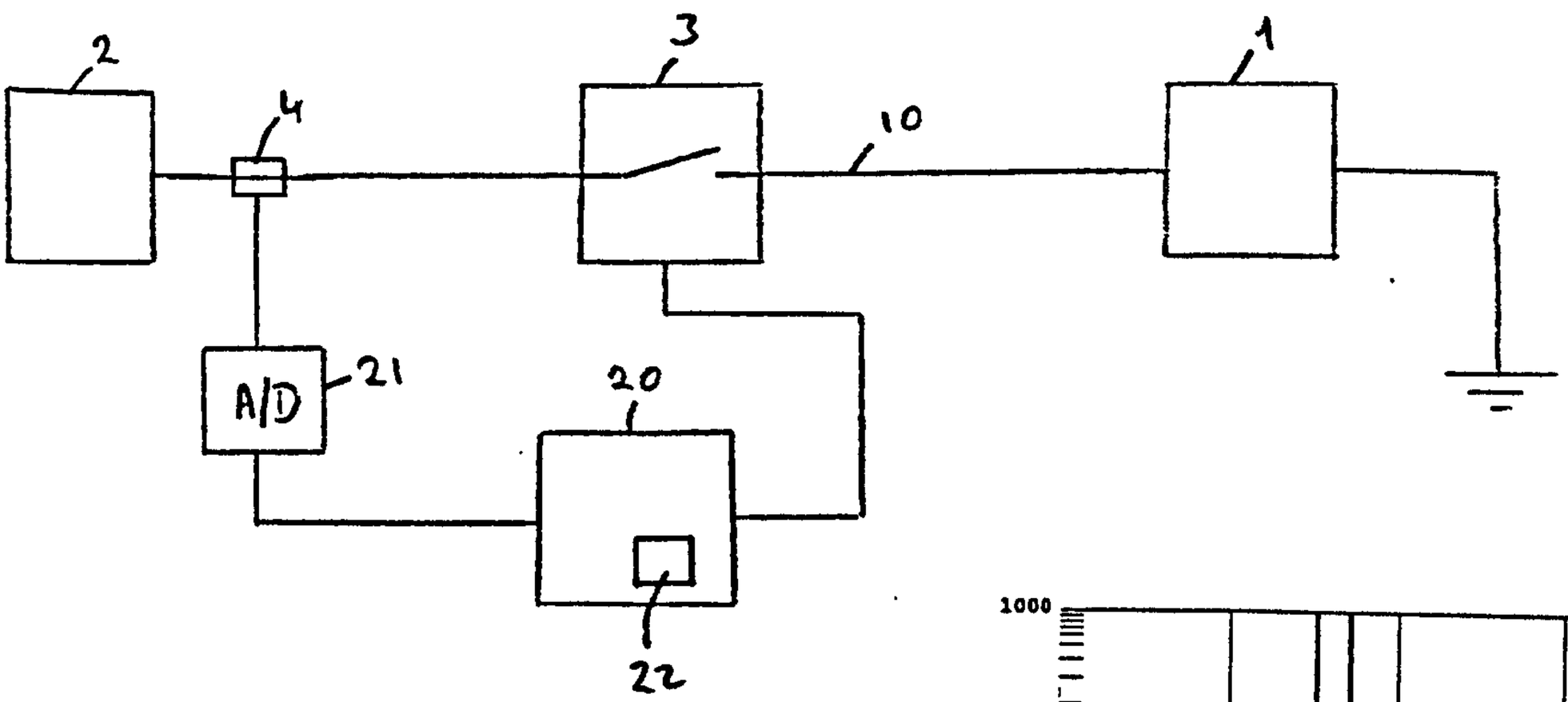


FIG. 2

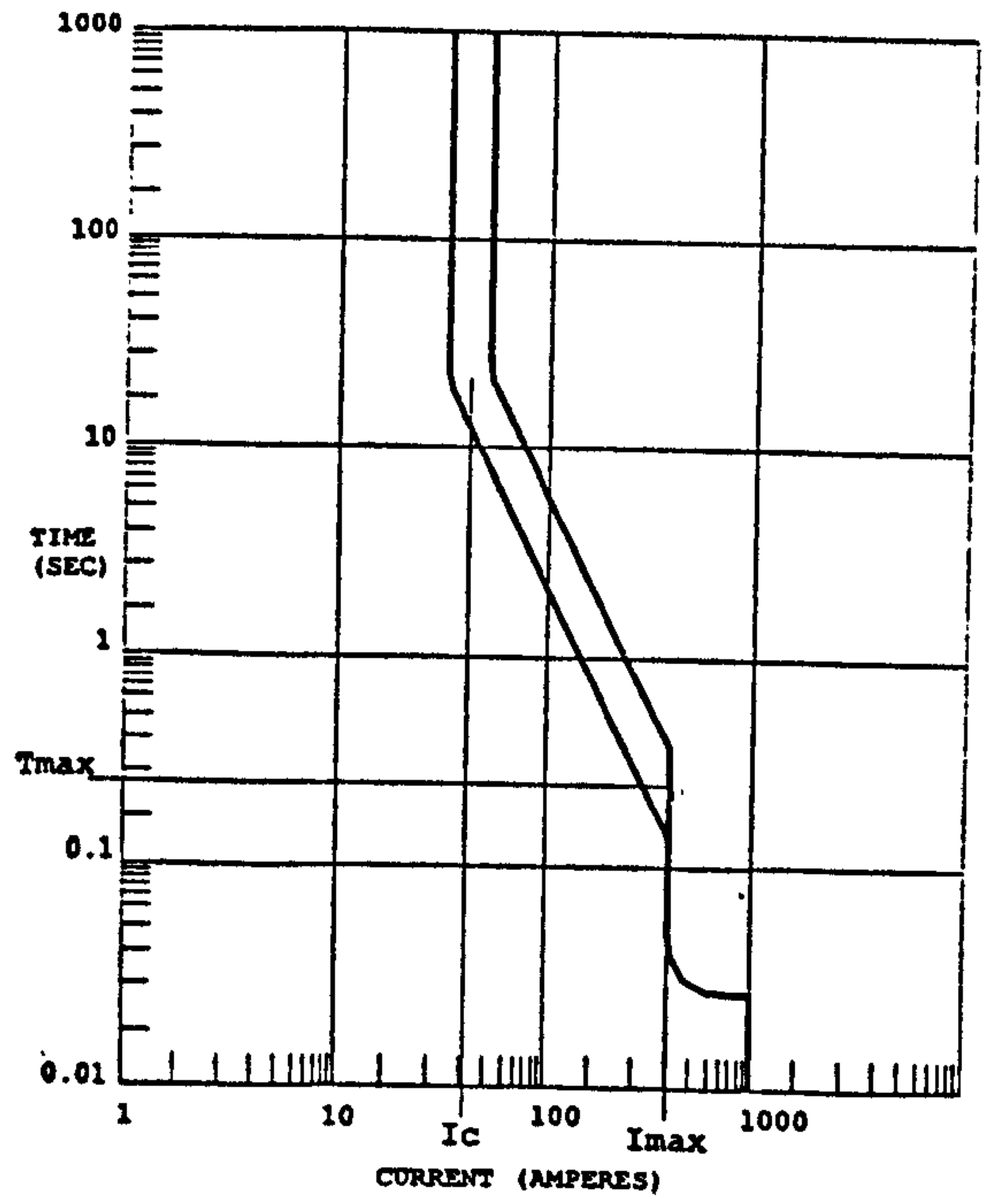


FIG3

Appendix 2:

Patent Application for Semiconductor Protection Trip Circuit

SMITHS INDUSTRIES

Aerospace • Medical Systems • Industrial

Internal Memorandum

From: **G.J. Kodish**
Location: **HQ**
Internal Tel No: **8241**
Facsimile No. **0181 201 8041**

Date: **26 July 1996**

To: K.P. Thomas - CH15
cc: R. Fitzpatrick - CH15

ELECTRICAL APPARATUS
9614590

The Patent Application for your "SEMICONDUCTOR PROTECTION TRIP CIRCUIT" was filed at the Patent Office on 11th July 1996 and given Application No. 9614590

A copy of the specification as filed is enclosed.

Gillian J. Kodish

ELECTRICAL APPARATUS

This invention relates to electrical apparatus and methods for controlling switching of circuit protection devices

The usual way of protecting electrical equipment and its wiring from current overloads is by means of an electromagnetic relay switch, thermal wire fuse or electrothermal circuit breaker. These previous arrangements, however, are usually relatively heavy and bulky. They also have a slow response time and can be unreliable in the long term. Because of this, there is a move towards using solid state power controllers (SSPC) employing power semiconductors, to switch electrical energy to a load and to interrupt current flow should an overload be detected.

The advantages of solid state controllers over electro-mechanical counterparts are well recognised and typically include factors such as reduced weight, reduced time to respond, increased lifetime and increased reliability.

Despite these advantages, using power semiconductors in such a role does require a great deal of care because of the adverse effect of high temperatures on semiconductor devices. The maximum temperature for devices made of silicon is about 175°C and for semiconductors made of silicon carbide it is about 400°C. In

current limiting SSPC's, the power density within each die may exceed 500W for short periods, resulting in rapid heating of the die and surrounding area.

It is an object of the present invention to provide apparatus for use in power switching and a method of controlling switching of a circuit protection device.

According to one aspect of the present invention there is provided electrical apparatus including a semiconductor switching device, means for deriving a measure of power dissipated by said device, means for providing a measure of the temperature in the vicinity of the device, and the apparatus being arranged to restrict flow of current through the device in response to a combination of said measure of power and said measure of temperature.

The apparatus preferably includes a processor arranged to calculate the resultant heat gain and heat loss of the semiconductor device in a short period of time, the processor being arranged to calculate the temperature of the device at the end of that time and to restrict flow of current through the device if the calculated temperature exceeds a predetermined temperature. Current flow through the device is preferably restricted by opening the switching device.

According to another aspect of the present invention there is provided a method of protecting a semiconductor circuit protection device comprising the steps

of measuring the temperature in the vicinity of the device, determining the temperature of the semiconductor device from the power dissipated by the device and a measured temperature, comparing the determined temperature with a maximum permitted temperature, and restricting current flow through device if the maximum permitted temperature is exceeded.

Electrical apparatus and its method of operation, in accordance with the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 illustrates the apparatus schematically; and

Figure 2 is a side elevation view of the semiconductor device in more detail.

The apparatus includes electrical equipment 1 and associated wiring 6 connected to a power source 2 via a solid state semiconductor device in the form of a power switch 3. The power switch 3 comprises a semiconductor die 30 secured to the top of a base substrate 31 by means of a bond layer 32. The substrate 31 may be arranged to act as a heat sink. The die 30 includes various electronic junctions used prevent or enable current flow through the switch. The switch 3 is encapsulated in the usual way. A current sensing device 4 supplies a signal proportional to the current

flowing through the power switch 3 and this is converted to a convenient digital form by means of an analogue-to-digital converter 9 at an appropriate regular sampling rate. A voltage sensing device 5 supplies a signal proportional to the voltage across the power switch 3, this being converted to digital form by the analogue-to-digital converter 9.

A temperature sensing device 10 is mounted by means of an adhesive, or the like, to the underside of the base substrate 31 and supplies a signal proportional to the temperature of the power switch 3. The temperature sensor 10 cannot be mounted directly at the semiconductor junction, which is the region most susceptible to excessive temperature, so it only provides a temperature signal representative of the temperature in the vicinity of the relevant part of the device. This temperature signal is converted to digital form by means of the analogue-to-digital converter 9.

The analogue-to-digital converter 9 could be implemented as three separate devices or it may comprise a single analogue-to-digital converter with a multiplexing arrangement to enable more than one signal to be converted. Each output sample of the analogue-to-digital converter 9 is used as a new data input to the processor 15, which calculates the temperature at the junction of the semiconductor die 30 from the power dissipated in the switch 3 and the temperature in the vicinity of the junction, as indicated by the output of the temperature sensor 10. More particularly, the processor 15 carries out the following steps in turn for each new data value:

1. Calculate the gross power dissipation within the solid state semiconductor switch 3 as a function consisting of the product of the digital representation of the current flowing through the power switch 3 and the digital representation of the voltage across the switch 3. It may be convenient to use a look-up table to perform this calculation or to scale the inputs or result using an appropriate scaling factor.

2. With the digital value representing gross power dissipation used as an input calculations conforming to equation 1 are now performed :

$$T_i^{p+1} = \left(q_i + \sum_j \frac{T_j^p}{R_{ij}} \right) \frac{\Delta t}{C_i} + \left(1 - \frac{\Delta t}{C_i} \sum_j \frac{1}{R_{ij}} \right) T_i^p \qquad \text{- (1)}$$

where

T is the calculated temperature of the node.

qi is the power delivered to node.

R_{ij} is the thermal resistance between two adjoining nodes.

C_i is the value of thermal capacitance for the node.

Δt is time step.

$p+1$ is the index indicating the predicted temperature at the end of the time step.

p is the index indicating the temperature calculated for the previous time step.

The node of interested is designated with the subscript "j" and the adjoining node with the subscript "i"

The semiconductor structure is decomposed into a matrix of volume elements, where each volume element can be viewed as a node which is connected by thermal resistance's to its adjoining neighbours.

Global assembly of equations conforming to Equation (1) are used to estimate the temperature of the semiconductor switch at discrete points in its structure. At a suitable point in the semiconductor nodal decomposition the calculated temperature T_j' is substituted by the converted value of temperature given by the temperature sensing device, thus providing a reference temperature of the ambient temperature conditions.

3. Compare the node with the maximum temperature to the maximum permitted temperature.

4. Command the semiconductor protection device 3 to open, halting current flow to the electrical load 1 if the node with the maximum temperature exceeds the permitted temperature.

The above method estimates the maximum temperature of the junction of the semiconductor protection device structure using the finite difference technique. Alternatively, the method of temperature estimation could be implemented using the finite element or transmission line matrix techniques.

The processor 15 could be a microprocessor or microcontroller. Alternatively, the processor could be implemented by dedicated or programmed logic devices connected in a circuit.

Although the above techniques can function satisfactorily, because they operate iteratively, the accuracy and continuous nature of its operation is dependant on the program execution time. Depending upon circumstances, it may be necessary to implement an additional control mechanism to the semiconductor protection device 3 to limit damage in the event of very high current. Similarly, depending upon circumstances, it may be desirable to input information from other sensors or information via a suitable interface, which the processor will consider to modify its control to the semiconductor switching device. An example of this would be a temperature sensor strategically located next to the load, which could be used to modify the amount of power supplied to the load in the event that the load temperature exceeds pre-set limits. An alternative example would be information from another controller.

When an excess temperature is detected, it may not be necessary in every application to open the semiconductor switch 3 in order to protect, since it is only necessary to restrict power dissipated by the device to a safe level. This could be done by reducing the current, such as by connecting a resistive component in shunt with the device, by removing some of the load, by using the semiconductor switch to limit the current, or by other means. Alternatively, the current flow through the device could be completely prevented by opening some other switch, or fuse, in series with the semiconductor devices.

It may also be desirable for the processor to be provided with a suitable interface to communicate information known to it, for example present current flow, voltage across the semiconductor protection device, power dissipated within the protection device, status - on, off, tripped etc., to external systems for more comprehensive system control.

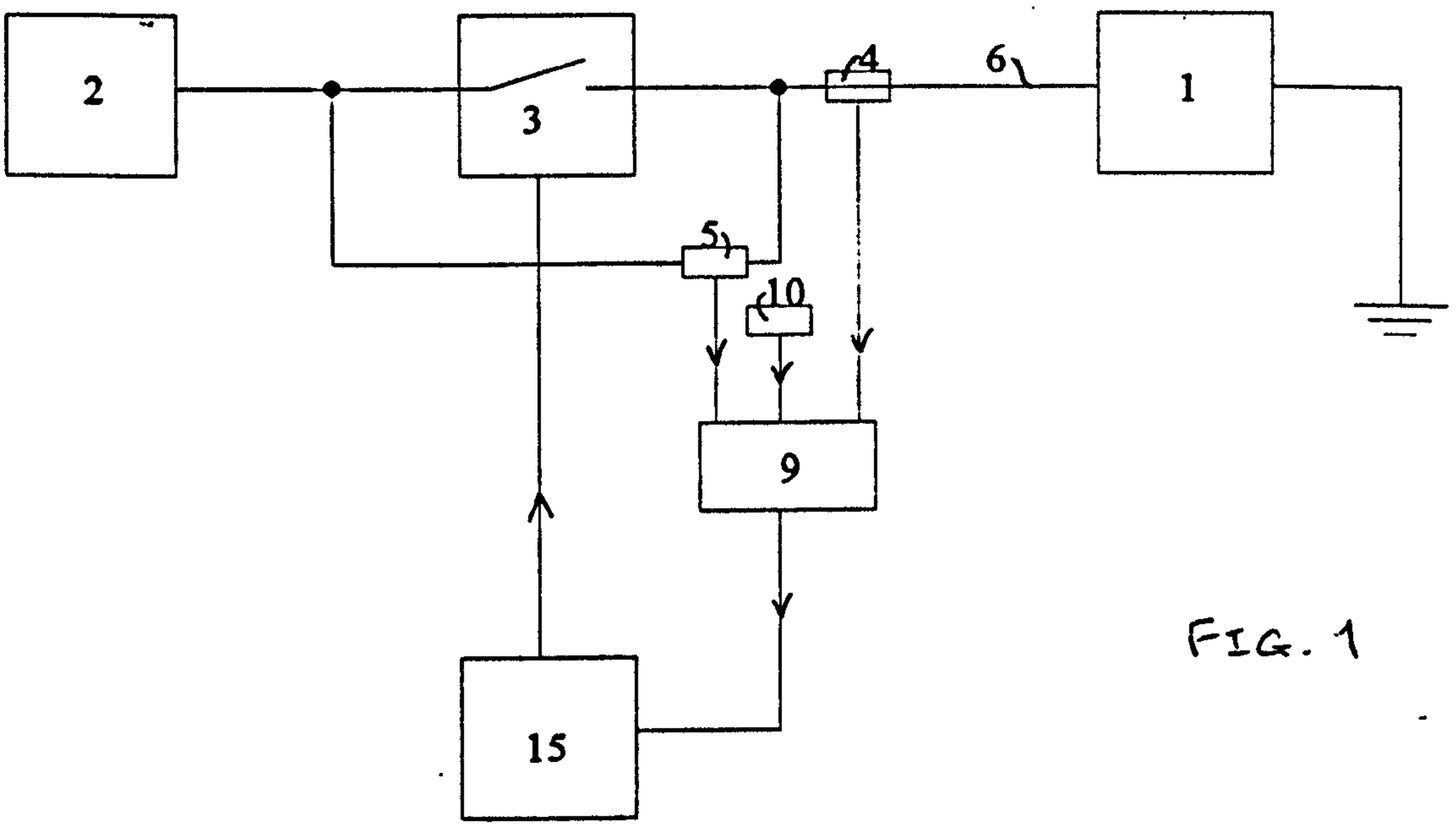


FIG. 1

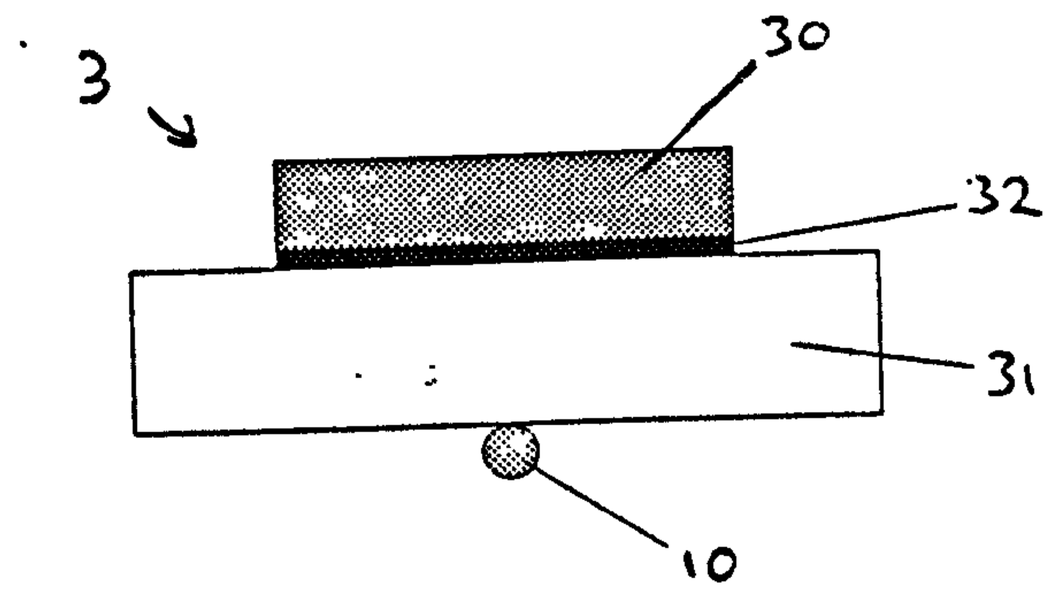


FIG. 2

Appendix 3:

Patent Application for Power Control Connector

SMITHS INDUSTRIES

Aerospace · Medical Systems · Industrial

Internal Memorandum

From:	**Jonathan Flint**
Location:	**HQ - Patent Dept**
Internal Tel No:	**8220**
Facsimile No.	**0181 201 8041**
Date:	**24 January 1995**

To: **Mr K. Rawlings - Cheltenham**

c.c. **Mr P. Thomas - Cheltenham**

POWER CONTROL CONNECTOR
PATENT APPLICATION REF: 9406625

I shall be grateful if you will please sign and return the enclosed forms, which I need for the French, German and US patent applications to be filed on this invention.

JONATHAN FLINT

ELECTRICAL SYSTEMS AND CONNECTORS

This invention relates to electrical systems and connectors.

In systems comprising a power supply and electrical equipment connected with the supply it is often necessary to monitor the equipment, such as its power dissipation, in order to detect a malfunction. In conventional systems, the power supply may include a distribution panel in which the monitors are contained, and power cables extending between the panel and the equipment. It will be appreciated, in such systems, that separate cables are needed for connecting the equipment to the panel if the equipment is to be monitored individually. Also, if individual equipment is to be isolated, such as on detection of a failure or for load shedding purposes, this requires each item of equipment to be connected to the distribution panel via an individual cable. Such systems require a large amount of wiring leading to complex installation and a heavy weight. By contrast, in power bus systems, where equipment tap off a common power bus, there is a much greater simplicity of installation and a reduction in the weight and volume. However, in power bus systems the monitoring, control and isolation of individual equipment has not previously been readily possible.

It is an object of the present invention to provide an improved electrical system.

According to one aspect of the present invention there is provided an electrical system including a power supply system including a control unit and a power bus, a plurality of items of electrical equipment, and a plurality of connector assemblies connecting each respective item of equipment to the power bus, each connector assembly including a power switch for

controlling supply of power to the associated equipment, a monitor arranged to monitor operation of the associated equipment and signalling means for interconnecting the control unit with both the power switch and the monitor so that the power switch can be controlled by the control unit in response to the monitor.

According to another aspect of the present invention there is provided an electrical system including a power supply system including a control unit and a power bus, a plurality of items of electrical equipment, and a plurality of connector assemblies connecting each respective item of equipment to the power bus, each connector assembly including a power switch for controlling supply of power to the associated equipment, means for reading configuration data of the associated equipment and signalling means for interconnecting the control unit with both the power switch and the configuration reading means so that the control unit can identify the configuration of each item of equipment and control its power switch accordingly.

An electrical system, in accordance with the present invention, will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 illustrates the system schematically; and

Figure 2 shows a part of the system in greater detail.

The electrical system may be installed in a vehicle, such as a car, aircraft, fighting vehicle or ship, or it may be installed in a factory or a house. The electrical system comprises a power supply system 1 having a power source 2, a power supply line 3 and a return line 4 connected to the source. The lines 3 and 4 run along the system to form a power bus and, running alongside this is a power control interface bus 5. The interface bus 5 is connected to a control unit 6.

Connected to the power bus 3, 4 and interface bus 5 are several items of electrical equipment, only three of which are shown here labelled 10, 20 and 30. In an aircraft, for example, equipment 10 might be the aircraft galley equipment, equipment 20 might be cabin lighting and equipment 30 might be the flight control computer. The equipment 10, 20 and 30 are connected to the power and interface buses by respective connector assemblies 11, 21 and 31. The connector assemblies 11, 21 and 31 each comprise a cable 40 and a connector 41 and 42 at opposite ends of the cable. The cable 40 has three wires 43 to 45 connected respectively to the power line 3, the power return line 4 and the power control interface bus 5, via the connector 41, which may be of conventional construction. The connector 42, at the equipment end of the assemblies 11, 21 and 31, is of a novel construction. In the present embodiment it is shown as being a female connector with an outer metal shell or housing 46 having three sockets 47, 48 and 49 at one end. The sockets 47 to 49 are arranged to receive corresponding pins 50 to 52 in a male connector 54 on the equipment 10, 20 and 30. The housing 46 of the female connector 41 is provided with conventional locking means (not shown) such as a locking ring, for retaining it on the male connector 54.

Within the housing 46 of the connector 42, the socket 48 is connected directly to the wire 44 extending to the power return bus 4. The socket 47 is connected to the power supply

line 43 via a power switch 60 within the housing 46. The power switch 60 may be an electromagnetic relay or a semiconductor switching device or circuit that can be externally controlled to prevent or enable supply of power to the socket 47. The housing 46 contains a power supply unit 61 connected across the power supply line 43 and the return line 44 on the side of the power switch 60 remote from the equipment. The power supply unit 61 derives power for the devices within the connector. The housing 46 of the connector 42 also includes a control and interface unit 62 connected to the power switch 60 by a line 63. A monitor unit 64 within the housing 46 is connected to receive an output from the power switch 60. The output is indicative both of the state of the power switch 60, ON or OFF, and of the power drawn by the associated equipment, such as derived from a current sensor in the power switch. The output to the monitor 64 may also include a signal representative of temperature of the power switch 60 so that the monitor is responsive to any overheating of the switch. The output of the monitor unit 64 is connected via a line 65 to the control and interface unit 62. The control and interface unit 62 is also connected to the third socket 49 of the connector.

The third socket 49 mates with the pin 52 in the equipment connector 54, which is connected to a configuration codes device 65. Although the third socket 49 is shown as a single socket, in practice, it might formed by several sockets or by several contacts in a single socket. The configuration codes device 65 may take many different forms such as, for example, an electronic store, a hard-wired connection of different pins or, a device such as a resistor of a selected value. The purpose of the configuration codes device 65 is to provide information about the nature of the equipment, such as, for example, its load and power requirements and its loads shedding priority. In the present example, the device 65 in equipment 10 indicates that it has a power requirement of 2000VA, that it is galley equipment and that, if load needs to be shed, it has a low priority. The device 65 in equipment 20 indicates that it has a power requirement of 300VA, that is a cabin lighting and that it has an intermediate priority. The device 65 in equipment 30 indicates that it has a power requirement of 100VA,

that it is the flight control computer and that it has a high priority. The configuration code device 65 may be included in the equipment connector 54 or at any other part of the equipment 10, 20 and 30.

In normal operation, the connector assemblies 11, 21 and 31 connect the equipment 10, 20 and 30 to the power supply source 2 and the control unit 6. The control unit 6 provides a continual monitoring for any malfunctioning of the equipment 10, 20 and 30 or the power switch 60 associated with the equipment. If any malfunction should occur, such as an excessive load being drawn by the equipment, a faulty opening of the power switch, or an overheating of the power switch, this will be signalled by the monitor unit 64 and the control and interface unit 62 via the power control interface bus 5 to the control unit 6. The power control unit 6 may respond, for example, to an excessive load being drawn by equipment 20 by supplying a signal on the interface bus 5 instructing opening of the power switch 60 in the connector 42 connected to the faulty equipment. This signal will be received by the control and interface unit 62 in all three connectors but only the unit with the correct configuration code will act on the instruction.

Similarly, there may be a fault in the power source 2 resulting in a reduction of the available power to a level insufficient to power all three items of equipment. In these circumstances, the control unit 6 identifies the equipment with lowest priority, namely equipment 10, and instructs the power switch 60 associated with that equipment to be opened so that power supply to the equipment is prevented and the overall power drawn by the electrical system is reduced.

The monitor unit 64 could also be arranged to open the power switch 60 directly, on detecting of a malfunction, without the intervention of the control unit 6. The monitor unit 64 and power switch 60 need not be separate units, as shown, but could be within a common unit.

Instead of locating the power switch 60, monitor 64, interface unit 62 and supply unit 61 within the connector 42, which mates with the equipment, they could be in the connector 41 at the other end of the assembly 11, 21, 31.

The interface bus 5 need not be a separate wire, as described above, but it could be provided on one of the power supply lines 3 or 4 by signals at a frequency different from the power supply frequency. In such an arrangement, the power control interface signals would be supplied to the control unit 6 and the interface unit 62 by appropriate filtering of signals on the power supply lines. Instead of using an electrical wire to provide the power control interface signals, these could be supplied via a fibre-optic cable. Alternatively, wireless techniques could be used, such as, an infra-red link or radio transmission.

The present invention enables considerable flexibility in the electrical system because the equipment can be connected to the bus at any point. Because the equipment do not have to be connected to the power supply source by dedicated cables, it considerably facilitates installation and reduces the amount of cabling required, thereby reducing the space requirement for the cabling and the weight.

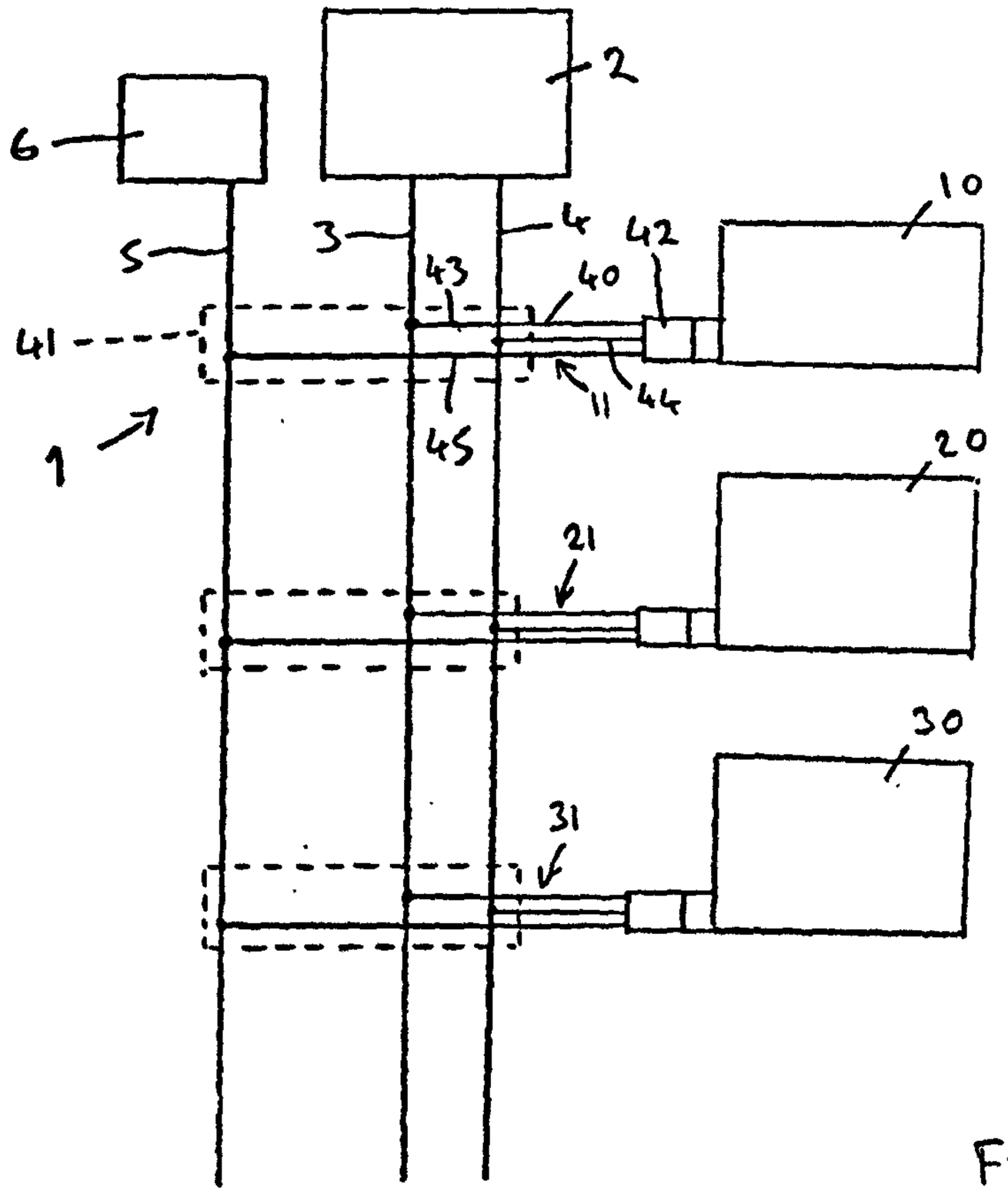

2
6
10
5
3
4
42
43
40
41
11
44
45
1
20
21
30
31

FIG. 1

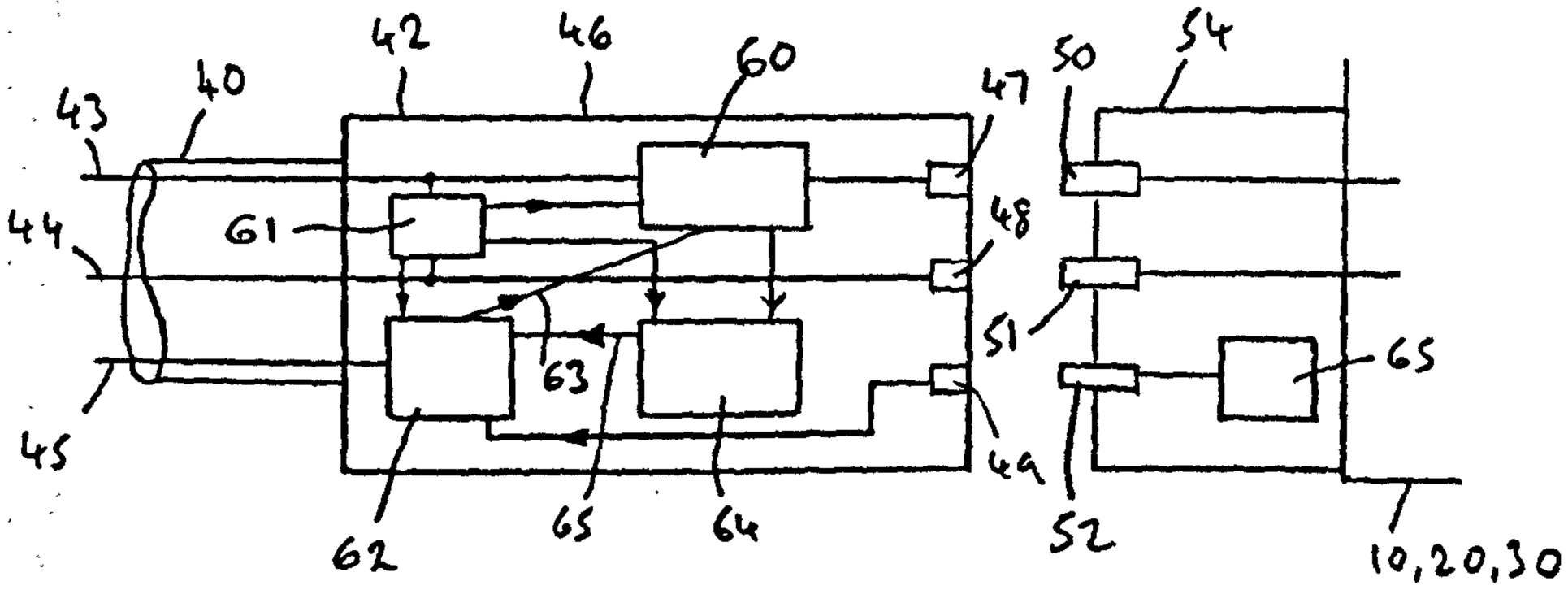

42
46
60
40
43
47
50
54
44
61
48
51
63
65
45
49
52
62
65
64
10,20,30

FIG. 2

Appendix 4:

Paper Presented at the 'New Developments in Power Semiconductor Devices' Colloquium, IEE, Savoy Place London.

Friday 21st June 1996.

Paper Title: 'Transient Thermal Impedance Measurement in Power Semiconductor Devices'.

IEE Digest Number: 1996/146.

Transient Thermal Impedance Measurement In Power Semiconductor Devices

K.P. Thomas, Smiths Industries Aerospace Ltd
Dr P.W. Webb, University of Birmingham

1. Introduction

Since the useful life of a power semiconductor device is greatly affected by the operating temperature in the application, good thermal characteristics in both steady state and transient conditions must be assured. For applications, like linear voltage regulators where the dissipation is approximately constant, the steady state thermal resistance of the package is sufficient to characterise the design. In switching applications however, where the dissipation may be characterised by short pulses of high dissipation, the thermal resistance of the package and the average dissipation will not completely characterise the thermal behaviour of the device.

To accommodate such applications where the device is subject to high power transient dissipation it is usual for the manufacturer of the power device to provide additional thermal information relating to its pulsed capabilities. As such, the "Transient thermal response curve" is the key tool provided by the semiconductor manufacturer to calculate peak junction temperatures.

This paper first examines the method widely used by semiconductor manufacturers to generate the transient thermal response curves. It then goes on to examine the validity of such curves by means of measuring the die temperature rise under pulsed power conditions using an infrared camera and by generating a comprehensive thermal model of the semiconductor device and package. The results are finally presented and conclusions are made.

2. Power Semiconductor Thermal Model

Most modern commercially available power semiconductors (MOSFET's IGBT's etc.) have a die mounting arrangement within its package similar to that seen in Figure 1.

In its most elementary form it consists of three components: a silicon die, a thin layer of die attach material and a base, which, depending on the package type may be made up of one or more layers of material.

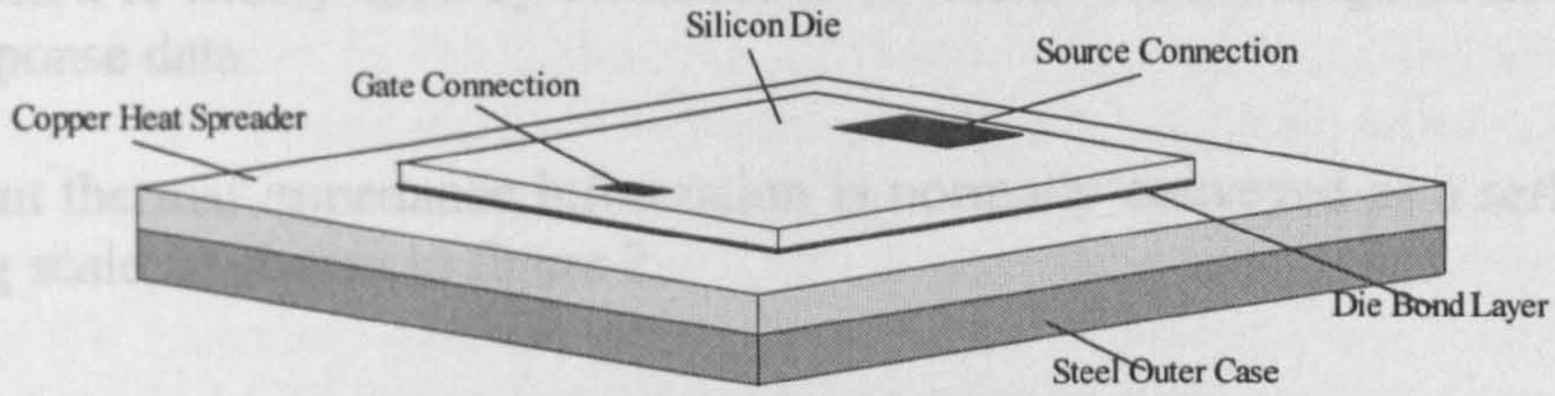


Figure 1 Die Mounting Arrangement (TO 3 Package)

Heat in the die is dissipated in any resistive path through which current flows. The dominant region of heat dissipation is in the die epitaxial layer, which is an area located directly under the top surface metalisation. The epitaxial layer is the active part of the device (the junction) and in most commercial devices occupies a depth of between 8 and 100uM [1] (the depth of the epitaxial layer increases with increased device voltage rating).

The traditional model widely used by semiconductor manufacturers to generate their transient thermal response curves assumes the heat is generated in an infinitely thin layer on the die top surface of the die. It also assumes a semi-infinite solid with uniform initial temperature within its volume. The problem has been analysed in detail by Carslaw and Jaeger [2] who give the following expression for the front surface temperature:

$$\Delta T = \frac{1}{\rho c\sqrt{\pi\alpha}} \int_0^t P(t-\tau) \frac{e^{-(x^2/4\alpha\tau)}}{\sqrt{\tau}} \delta t \quad \text{- (1)}$$

where: P(t) is the power function within the infinitely thin layer, τ is the variable of integration, α is the thermal diffusivity of silicon (47.53mm^2/sec), ρ is the silicon density (2.4 10^{-6} Kg/mm^3) and c is the specific heat capacity of silicon (736.4 W sec/Kg K)

Since we are only interested in the peak temperature, this expression becomes:

$$\Delta T = \frac{1}{\rho c\sqrt{\pi\alpha}} \int_0^t \frac{P(t-\tau)}{\sqrt{\tau}} \delta t \quad \text{- (2)}$$

This can be solved for specific power functions i.e. rectangular, triangular etc. For a rectangular power function the peak surface temperature is reached at the end of the pulse and is given by the following expression:

$$\Delta T = \frac{P_0}{\rho c\sqrt{\pi\alpha}} \int_0^t \frac{\delta t}{\sqrt{\tau}} = \frac{2P_0}{\rho c\sqrt{\pi\alpha}} \sqrt{\tau} \quad \text{- (3)}$$

where P_0 is the peak value of the power pulse.

This expression is widely used by semiconductor manufacturers to generate the transient thermal response data.

The transient thermal impedance information is normally conveyed as a series of curves on a log/log scale, as shown in figure 2.

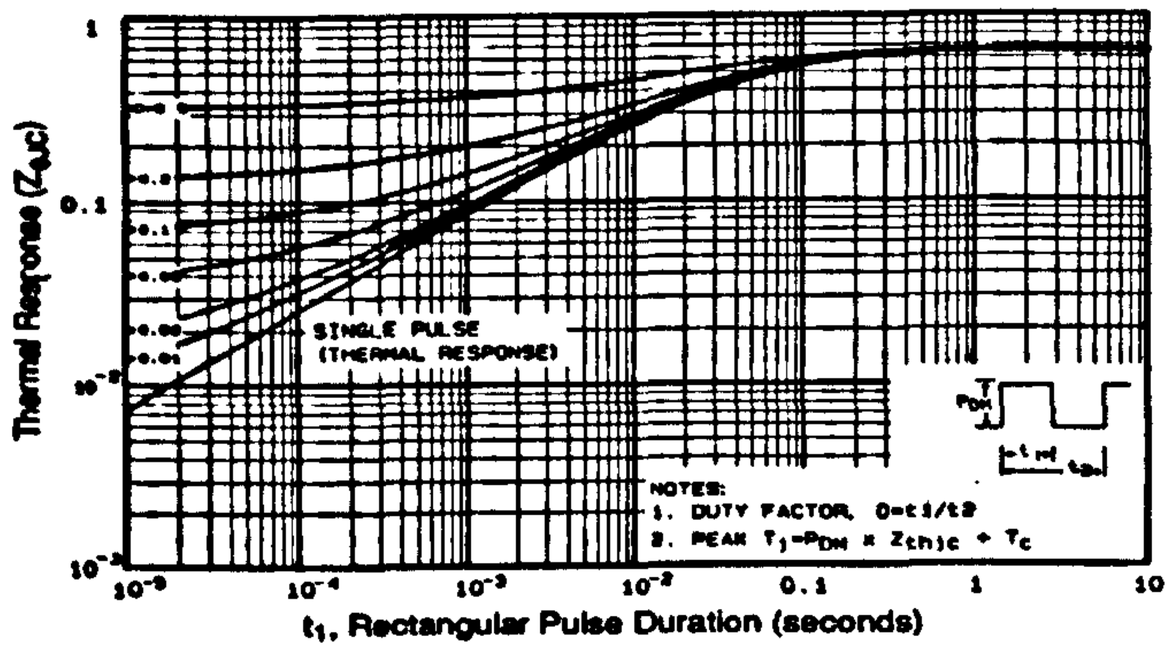


Figure 2 Example Manufacturers Transient Thermal Impedance Curve

The x axis displays the time duration of a rectangular pulse of dissipated power and the y axis displays the transient thermal impedance junction to case (Zth_{jc}). The series of curves relate to whether the dissipation pulse is singular or a continuous train, therefore each curve displayed relates to a specific duty cycle.

To calculate the peak junction temperature following the dissipation of a rectangular power pulse (P_{DM}) for a time duration (T_1) one can lookup the pulse duration on the x axis and where it intersects the appropriate curve, read from the y axis the value of Zth_{jc} corresponding to the pulse duration. Given the value of Zth_{jc} the peak junction temperature may be calculated as follows:

$$Tj\ (Peak) = P_{DM} * Zth_{jc} + Tc \qquad -(4)$$

where Tc is the initial junction temperature.

3. Transient Thermal Impedance Measurement

To assess the accuracy of the model used by the device manufacturer to produce the transient thermal impedance information a detailed study was undertaken to determine die heating characteristics under controlled conditions. The approach taken with the study was twofold: to measure die temperature under varying levels transient power by means of a IR thermal imaging camera and to develop a detailed numerical thermal model of the test subject using a specialised computer modelling tool. Two devices were chosen as test subjects, both power MOSFET's namely IRF044 [3], IRF054 [4].

3.1 Temperature Measurement

The Wolfson Laboratory in the University of Birmingham provided the test facility for the MOSFET die temperature measurements. Prior to performing any transient temperature measurements on an 'open can' device however, it was first necessary to measure the die temperature under steady state conditions. This was performed using an Agema 900 XY scanning microscope. Such a measurement was necessary in order to confirm the sample MOSFET was free from any defects in the die bonding which could account for a higher than normal reading. The measurements also served as a means of determining the true value of the device junction to case thermal resistance (Rth_{jc}) and assisting in the construction of a thermal numerical model.

The transient temperature measurements were performed using a Barnes RM2 spot microscope based on an InSb liquid nitrogen cooled detector. The time constant of this detector is 1μS allowing transient heating in excess of this time to be recorded. A control circuit connected to the MOSFET enabled a precise level of power to be dissipated in the die for a finite time period. A number of measurements were taken with power dissipation levels ranging from 500 to 2000 Watts. Figure 3 shows one such temperature recording overlaid with the theoretical (modelled) temperature rise.

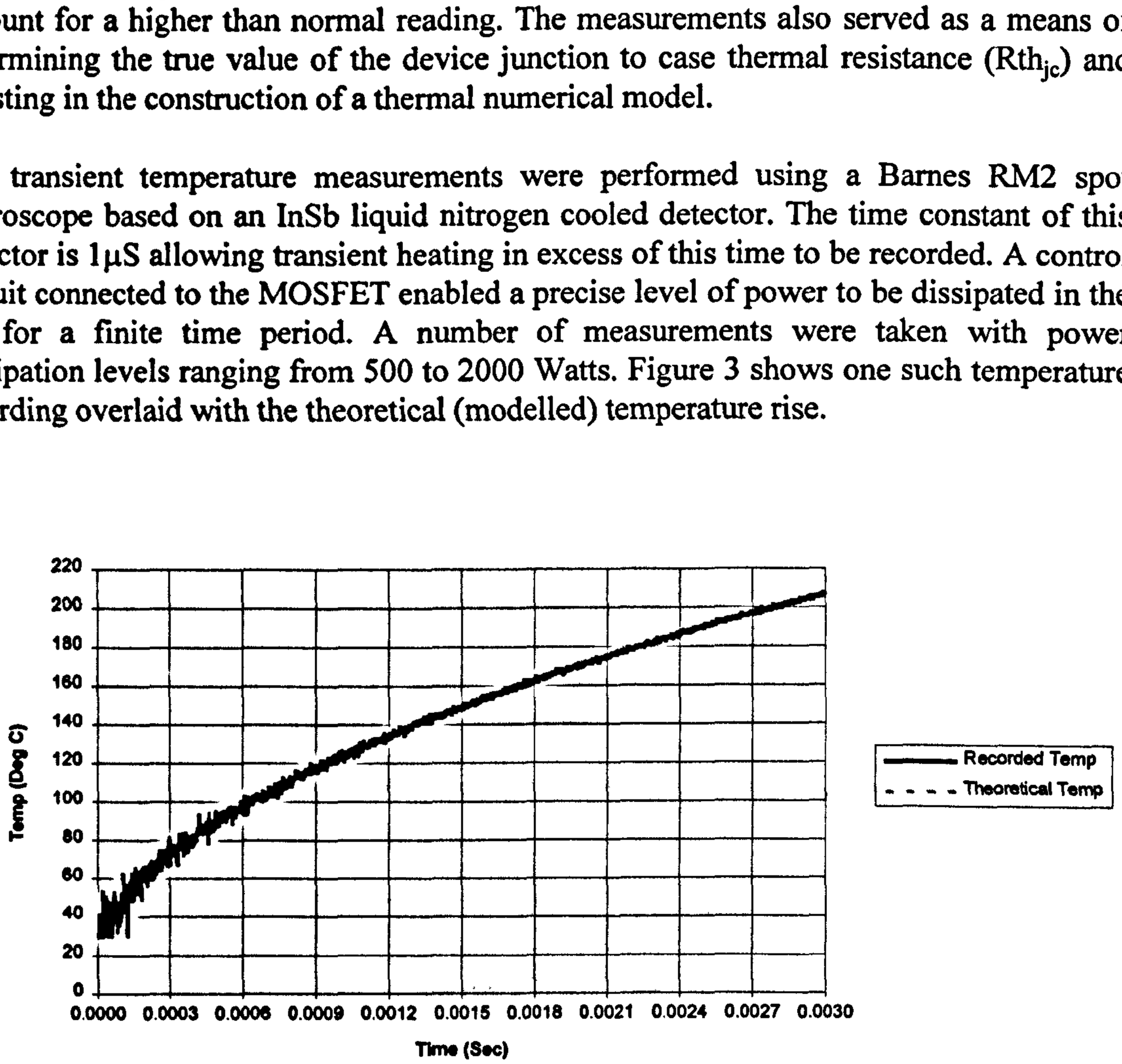


Figure 3 Measurement Trace IR044 1000W Dissipation

3.2 Thermal Modelling

A detailed thermal model was constructed of each device under test in order to characterise the die heating for incremental levels of power between 50 and 2000W (taking such a large number of readings would have impractical using the IR microscope). The modelling tool used for this activity was based on the 'Transmission Line Matrix' technique [5]. The model was constructed from the data provided by

sectioning the devices and measuring the physical dimensions and the material properties. The final model produced results in accordance with both the steady state and transient IR measurements.

4. Results

Using the results from this modelling activity together with the empirical temperature measurements obtained with the IR microscope it was possible to plot a comparison with the values obtained from the manufacturers transient thermal impedance curve. Figures 4 and 5 shows this comparison.

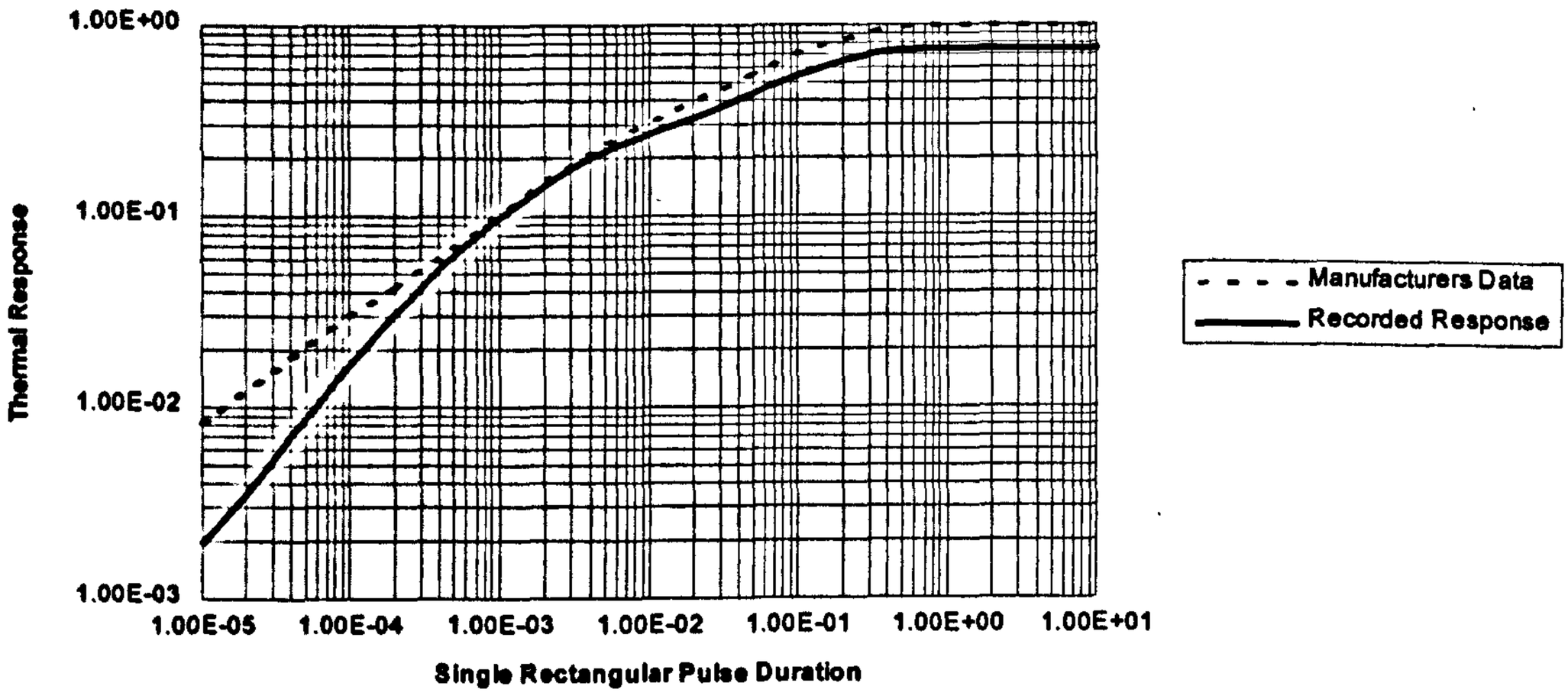


Figure 4 IRF 044 Transient Thermal Impedance Comparison

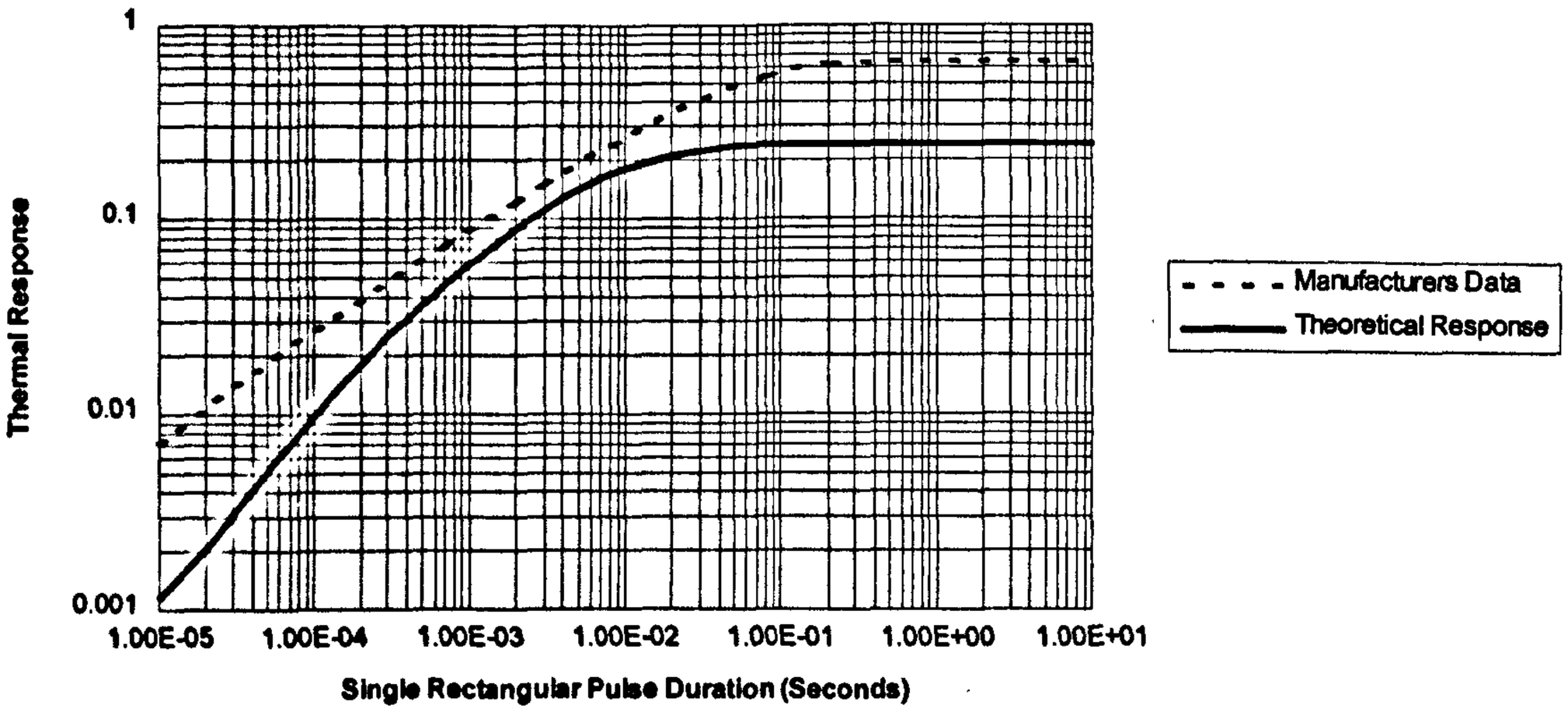


Figure 5 IRF 054 Transient Thermal Impedance Comparison

5. Conclusions

From the results presented it is obvious the transient thermal impedance curve obtained through measurement and modelling differ significantly in both devices from the curve provided by the device manufacturer. The most prominent deviation occurs either when the pulse duration is very short i.e. <.0001s or where it nears and reaches its final steady state value.

A possible explanation for the large discrepancy experienced where the pulse duration is very short could relate to one of the assumptions used in equation (3) i.e. 'the power is dissipated in an infinitely thin layer at the surface of the die'. In practice, as has already been mentioned the active region where power dissipation occurs is a significant fraction of the thickness of the die and this assumption has no justification, other than analytical expediency. Since the power in reality is dissipated in layer of finite thickness the temperature rise for a given level of power will not be as large owing to the increased volume of the dissipation area. This results in the lowering of the Zth_{jc} value as shown in both curves. The discrepancy in results for long pulse duration's relates to the difference in the steady state Rth_{jc} value provided by the device manufacturer and the measured /simulated value obtained from the investigation. In the case of the IRF054 the manufacturers figure is over twice that of the value realised by experimentation. The author can only surmise a large contingency is allowed by the manufacturer to account for variations in the production process e.g. die solder bond thickness varying or voids being present in this solder bond. In reality the batch devices dissected were found to be consistent and of high uniformity.

6. References

1. Clemente, S. 'Transient thermal response of power semiconductors to short power pulses'. IEEE Transactions on Power Electronics Vol 8 issue 4 P.337-41, Oct 1993

2. Carslaw, H.S and Jaeger, J.C. 'Conduction of Heat in Solids'. Second Edition Oxford University Press 1959.

3. HEXFET Power MOSFET Designers Manual, Volume 3, International Rectifier September 1993.

4. HEXFET Power MOSFET Designers Manual, Fourth Edition, International Rectifier 1987.

5. Webb, P.W and Gui, X. 'Implementation of Timestep Changes in Transmission - Line Matrix Diffusion Modelling'. International Journal of Numerical Modelling, Vol.5 pp 251 - 257 (1992).

Appendix 5:

Paper Submitted to the IEE Proceedings, Electric Power Applications and Explanatory Covering Letters.

Paper Title: 'Digital Implementation of Overcurrent Protection Circuit Breaker Characteristics for Solid State Protection'.

SMITHS INDUSTRIES
Aerospace

Bishops Cleeve
Cheltenham
Glos., GL52 4SF
Telephone: 0242 673333
Telex: 43172
Fax: 0242 661_ _ _

12/9/96

Direct: 0242 661311
Fax: 0242 661111

Dr Paul Webb
Department of Electrical Engineering
University of Birmingham
Edgebaston
Birmingham

Dear Dr Webb,

Re paper: "Digital Implementation of over-current circuit breaker characteristics for Solid State Protection"

The above paper was written by Paul Thomas and submitted to the IEE journal, Electrical Power Applications earlier this year. At the time of submission, Smiths Industries, did not have any problems with the publication of this material.

However, one of the major business divisions within Smiths Industries requested that publication should be stopped and Paul has been instructed to withdraw the paper. The reason for this is that the business division have informed us of their plan to exploit this technology with a business partner and did not wish any publication of the technology. The product area that this technology will enhance could represent some 25% of Smiths Industries Aerospace group turnover by the turn of the century and is therefore of great significance.

Yours sincerely,

Keith Rawlings
Central Research

SMITHS INDUSTRIES
Aerospace

Bishops Cleeve
Cheltenham
Glos., GL52 4SF
Telephone: 01242 673333
Fax: 01242 661111

CH15 - RPT/KPT/DK
16 September 1996

Mr K Martin
IEE Proceedings
Electric Power Applications
Michael Faraday House
Six Hills Way
STEVENAGE
Herts
SG1 2AY

Dear Mr Martin

Submitted Paper Ref EPA.96/2168

Title: Digital Implementation of Overcurrent Protection
Circuit Breaker Characteristics for Solid State Power Protection

With reference to our recent telephone conversation, as you are aware Smiths Industries business position has changed with regard to the algorithms detailed in this paper. Since submission, Smiths Industries has agreed a major joint development with an overseas manufacturer for a product based on one of the algorithms contained in the paper and publication of the paper could compromise the Company's business interests. A patent has been applied for covering this intellectual property. If the patent is published in the next few months, Smiths would not wish the paper to be published until the patent cover has been confirmed.

In view of this I would be grateful if you would stop any possible publication until such time as I contact you again following the award of full patent cover. I am sorry for the inconvenience this will cause you and I trust the matter will be resolved in the near future. If you have incurred expenses in getting the paper referred, I am assured that the Company would look favourably on reimbursement.

Yours sincerely

K P Thomas
Smiths Industries Corporate Research

cc: Mr K A Helps
Dr K C Rawlings

DIGITAL IMPLEMENTATION OF OVERCURRENT CIRCUIT BREAKER CHARACTERISTICS FOR SOLID STATE POWER PROTECTION

By

K.P. Thomas

Smiths Industries Corporate Research

ABSTRACT

Continuing advances made to the performance of power semiconductor switching devices together with reductions in cost has now reached a stage whereby requirements for traditional electromechanical power protection and switching are being superseded by their solid state counterparts.

Although many benefits are to be gained by this transition, a problem still remains on how to provide the true current-squared-time (I^2t) wire protection to such products which are intrinsic to older electromechanical protection devices.

This paper examines the problem and contrasts two differing approaches to its solution, one approach being all analogue and the other digital. In the course of this discussion two algorithms are presented as a means of accurately implementing an I^2t trip curve using a low cost microcontroller.

1 INTRODUCTION

Until relatively recently the combination of the electromechanical relay and the thermal-electromagnetic circuit breaker has been dominant as a means of controlling the connection of power to electrical loads and protecting power sources, feeders and distribution wiring from hazardous current overloads. As the cost of power semiconductor devices has continuously fallen however, and the electrical performance of such devices consistently improved, power semiconductors are now forming the building block of Solid State Power Controllers (SSPC's) which combine the functions of power switching and protection within one device.

The advantages these solid state controllers have over their electro-mechanical counterparts are well recognised [1][2] and include factors such as reduced weight, size, response time, increased long term reliability, and real time status reporting. One problem faced by the designers of SSPC's however, is the complex issue of how best to implement the true current-squared-time (I^2t) wire protection trip characteristic which is intrinsic to the older thermal-magnetic circuit breaker.

This paper examines the requirement for true I^2t wire protection in solid state power controllers which are designed to work up to ac/DC voltages of 500V and discusses briefly the protection and co-ordination concepts applied to power distribution systems. As an aid to the understanding, attention is focused on the

simple mechanism thermal circuit breakers employ to perform this important function. The paper then goes on to contrast two differing approaches to solving the problem. One approach being to model the I^2t function as an analogue circuit and the other approach involves modelling the problem digitally. The merits and disadvantages of each method will be explored.

In the course of this discussion two differing software algorithms are presented, which offer the capability of accurately providing this I^2t function within an SSPC.

2 PROTECTION / CO-ORDINATION CONCEPTS

When an overload fault occurs within a power distribution system, overcurrent protection devices are used to isolate only the section of the system affected by the fault, so the remaining system can continue to operate normally. The device has the task of safeguarding the wiring to the affected load downstream of the protection device and equally protecting the power source upstream. Since faults can occur anywhere in the electrical system many protection devices are normally required. These devices are located such that a single device or, if necessary a combination of devices, operate to isolate a fault.

Good practice dictates that the isolated area must be as small as possible and only the device nearest the fault should operate to perform this task. In addition, the possibility of a protection device not working must be considered. If this happens, the next upstream device or combination of devices must operate to provide a co-ordinated backup protection. Time discrimination between successive devices provide the necessary means for this co-ordination of protection.

The protection device should have the attributes of safeguarding the system components from sustained overloads whilst being insensitive to the transient power demands experienced when powering loads such as motors or filament lamps from an initial off state (these devices typically require a starting current 7 or 8 times steady state current). To achieve this insensitivity the protection device should continue to deliver power under overload conditions for as long as it is safe to do so. The time it can maintain this overload current safely is dictated by the current rating and heating characteristics of the downstream wire the device is protecting.

OVERCURRENT CHARACTERISTICS

Thermal-magnetic circuit breakers like simple wire fuses have inverse time-current characteristics. This means the larger the overload current the shorter the time to trip. Such devices conform to the constant I^2t

which was recognised by G.J. Meyer in On the theory of fuses [3] and stated that ' I^2t is a quantity which is inherent in any metal'. It describes the energy capacity of a metal conductor with respect to the heating generated by an electrical current flowing through it. Hence, I^2 (the square of the current) represents a heating function and t represents the time to reach a critical energy level (trip time). The time lag inherent in the formulae is a function of the conductor material and its cross sectional area.

This constant however only represents part of the problem, since it is obvious the device would eventually trip at any non-zero current flow, whereas, the desired characteristic is that the device will never trip if the current is below a certain value. In a thermal circuit breaker or fuse this is achieved by allowing the heating element to lose a certain amount of heat to the surroundings which may be regarded as an infinite heat sink. The loss of heat can be considered to conform to the Newtonian cooling law i.e. :- 'the heat transmission across a surface can be considered proportional to its temperature rise above ambient'.

Thermal circuit breakers consist of a bi-metallic strip which bends when heated by the load current flowing through it. Continuous overload currents will cause the bi-metal to deflect and eventually to trip the circuit breaker. One can view the simple thermal circuit breaker as an analogue computer since if it is rated correctly to the downstream wire, it models the heating taking place within that wire (since all metals have an I^2t constant) and will trip when the wire temperature exceeds its thermal limit. Unfortunately this mechanism is not present in an SSPC and consequently must be synthesised using an appropriate technique.

3 ELECTRONIC REPRESENTATIONS OF THE I^2t CHARACTERISTIC

At present, current versus time curves are used to describe the operation of a protective device [4][5]. For a given circuit breaker (a 'standard' MS3320, 1 to 20A device will be used as an example) these characteristics are usually published as bands on a log/log graph as shown in Figure 1.

Figure 1 MS3320 Current versus Time to Trip Curve

The vertical axis represents the time to trip (normally in seconds), and the horizontal axis represents the load current either as an absolute value or a per unit overload 'PU' (i.e. actual current/nominal current). The band represents the bounds of acceptable behaviour and where a tolerance has been applied (this tolerance is due to inaccuracies caused by mechanical deficiencies and the effects of ageing [6]). The lower edge of the band indicates the minimum time duration at a specified current in which a device may initiate a trip. For all points below this, the device should never trip. The upper edge of the band indicates the maximum

time duration at a specified current for the device to initiate a trip. If one were to continue the slope of the curve so that it intersects with the 1 PU current line (see the fine line in Figure 1) the time read from the vertical axis at the point of intersection represents the thermal time constant of the protection device.

For an electronic I^2t circuit the problem of defining the device is this:-

This graphical method of specifying a protection device has been used for a great number of years, consequently all circuit breaker manufacturers provide trip curves for their circuit breakers in this format [7]. The electrical equipment manufacturers likewise are used to this method of specification and often detail their requirement for a wire protection device on the basis of what has been empirically found to be acceptable on previous generation equipment. It is highly probable therefore that the only design specification material the designer of the I^2t circuit will ever have is this current versus time trip curve.

The problem arises because in a sense the current versus time curve is only half a specification, in that it details quite precisely the steady state or overload response of the trip device, but contains no explicit information relating to what should happen when the device was subjected to a below trip overload, which has since gone away (i.e. as in the case of the inrush characteristic many loads exhibit when energised). This factor is important, since as previously mentioned the protection device should model the temperature of the downstream wire it is protecting. A previous non-trip current overload will raise the temperature of the wire above nominal for a period of time. Should a second sustained overload occur during this same period, then the protection device should trip in a shorter time than it otherwise would when subjected to just the second overload, since the downstream wire is already at a raised temperature. More fundamentally the trip times are derived empirically under test conditions where the device is subjected to an over current with no initial load [5]. In practice the device may already be conducting a steady state current when the overload occurs, as such the time to trip for the overload current will again be shorter because the wire temperature is already raised.

A thermal circuit breaker models this to the greater extent, since like the wire it is protecting it is made of a metal strip which when subject to heating by the overload current has a thermal memory similar to that of the downstream wire. An electronic solution built to implement a protection device specified using the time versus current curve could adequately meet the specification but offer poor protection in reality since it need not consider the thermal memory issue as the device specification has no explicit requirement [8]. A usable device must however both model the wire heating and cooling in order to provide the necessary degree of protection.

4 SIMPLE MODEL OF WIRE HEATING

As a first step in developing a solution to the I^2t problem it is necessary to create a general form describing the heating which takes place within a wire when it is carrying an electrical current.

Consider a wire of unit length carrying a current (I) for a time greater than zero ($t > 0$).

Its temperature at time t is:

$$Ta + \Delta T(t) \qquad \text{-(1)}$$

where Ta is the ambient (starting) temperature and ΔT is the temperature rise due to the electrical current.

clearly -

$$\Delta T(t) = CV \int_0^t (Pin - Pout).dt \qquad \text{-(2)}$$

where C is the thermal capacity of the wire material, V is the volume of the unit length of wire, Pin is the power into the wire and $Pout$ is the power out of the wire.

Pin is due to the resistive heating so

$$Pin = I^2 R \qquad \text{-(3)}$$

where I is the measure of current conducted within the wire and R is the resistance of the unit length of wire.

Pout is the heat loss to the surroundings due to conduction, convection and radiation. A simple model assumes the heat loss is proportional to the temperature rise of the wire above ambient.

If the wire temperature were at ambient at $t=0$ then

$$Pout = K\Delta T(t) \qquad \text{-(4)}$$

where K is the coefficient of heat loss.

Hence -

$$\Delta T(t) = CV\int_0^t \left(I^2R - K\Delta T(t)\right).dt \qquad \text{-(5)}$$

If I and R are constant -

$$\Delta T(t) = aI^2t - b\int_0^t \Delta T(t).dt \qquad \text{-(6)}$$

where $a = CVR$ and $b = CVK$ using the notation above.

The solution to this is -

$$\Delta T(t) = \frac{c}{d}I^2\left(1 - e^{-bt}\right) \qquad \text{-(7)}$$

where c and d are constants.

If c and d are known (which in reality would normally not be the case), the time to achieve a given temperature rise for a particular current (I) can be calculated. In practice however, a wire will be rated for a maximum continuous current which will result in a maximum temperature rise that can be tolerated before damage to the wire, or wire insulation will occur. Obviously it is the absolute temperature that can be tolerated that matters, therefore the maximum ambient operating temperature + the maximum temperature rise due to the current flow must not exceed this limiting temperature.

This situation is represented in the model by -

$$\lim_{t\to\infty}\{\Delta T(t)\} = \lim_{t\to\infty}\left\{\frac{c}{d}I^2\left(1-e^{-bt}\right)\right\} \qquad -(8)$$

consequently we have -

$$\Delta T\max = \frac{c}{d}\left(I_{rated}\right)^2 \qquad -(9)$$

Where $\Delta T\ max$ = the maximum allowable temperature rise, and I_{rated} is the maximum continuous current for the wire. The time to trip for current overload protection is the time taken to reach $\Delta T\ max$, therefore, substituting for ΔT(t) in equation 7 from equation 9 gives -

$$I_{rated} = I^2\left(1-e^{-bt}\right) \qquad -(10)$$

or

$$t = \frac{1}{b}\ln\left(\frac{1}{1-\left(\frac{I_{rated}}{I}\right)^2}\right) \qquad -(11)$$

Where *1/b* represents a time constant.

5 METHOD 1 - AN ANALOGUE SOLUTION TO THE PROBLEM

As previously discussed, any electronic implementation of the I^2t characteristic must not only provide the current overload versus time to trip characteristic graphically specified, but must also provide the thermal memory which is intrinsic to the thermal circuit breaker. Should this thermal memory requirement be ignored, the protection device could at best be prone to nuisance tripping or at worst offer potentially little protection to the wire.

It is interesting to note that equation 10 has the same form as:

$$V_C = Vi\left(1 - e^{-\frac{t}{rc}}\right) \qquad \text{-(12)}$$

which describes the voltage on a capacitor when a resistor - capacitor (*rc*) network is subjected to a unit step in voltage and where the time constant is given by the product of *r* and *c*. This suggests an implementation of an I^2t trip as follows:-

Figure 2 Analogue I^2t Implementation

The implementation given in Figure 2 uses an analogue multiplier to represent the energy fed into the downstream wire. The resistor capacitor network has a time constant matching the thermal time constant of the wire/thermal circuit breaker (this parameter as previously described is obtained from the time versus over-current trip curve - see Fig 1). The voltage generated across the capacitor represents the actual temperature of the downstream wire, and as such the circuit will issue a trip command if this capacitor voltage exceeds a threshold voltage representing the maximum allowable temperature the wire can reach (i.e. the square of the wire current rating). One important point regarding this circuit is that the capacitor's ability to store charge provides the necessary mechanism to satisfy the thermal memory requirement.

Despite the circuits simplicity, a practical implementation does however suffer from a number of drawbacks which have a direct impact on the circuit accuracy:

A conventional circuit breaker is usually specified to an overload current 1000% above its nominal rating [5] (on certain applications this can extend to 3000% [7]). This means the circuit can be expected to handle an input voltage 10 times greater than the voltage developed for a normal load current. If a voltage 10 times as large is input into the multiplier, then it is obvious since the multiplier is performing a squaring function it will yield a voltage 100 times as large at the output. The positive output voltage swing of most commercially available analogue multipliers (e.g. AD633JN, MPY634KP) are in the order of +11V, consequently the input voltage in relation to normal load current can only be 330mV maximum. The output of an analogue multiplier is prone to offsets of up to 50mV, thus representing a 15% error at 1000% overload and 45% at 3000%. Higher accuracy devices are of course available but the cost is significantly higher and would probably render any solution uneconomic.

The second problem relates to the resistor and capacitor values required to model the thermal time constant of the wire. In most applications this time constant is in the order of 8 to 25 seconds. Generating time constants of this magnitude using resistors and capacitors presents certain problems in that large value

capacitors are generally accompanied by either large size or poor tolerance. If the resistor value is instead increased to reduce the required capacitance, the capacitor dielectric leakage current becomes a significant factor and has the effect of distorting the model and making the wire appear cooler than it otherwise would be in reality.

6 METHOD 2 A DIGITAL SOLUTION TO THE PROBLEM

With continuing reductions in the cost of microprocessors, microcontrollers and programmable logic devices, a digital approach to characterising trip curves becomes an increasingly attractive option [10][11], both in economic terms and as a way to overcome the accuracy difficulties of an all analogue solution.

Consider the circuit previously given in Figure 2, the functionality of this circuit can be simply decomposed into a number of discrete operations, namely:

i, A squaring operation

ii, An integration

iii, A comparison and decision to trip.

All these functions are amenable to digitisation.

The first stage in the digitisation process is to capture the input voltage in a binary form, this is normally performed using an analogue to digital converter. The digital value can then be multiplied by itself to yield a value representing the load current squared. This numerical value will then serve as the input into the following algorithm which provides the required first order lag :-

At time (t) the temperature of the wire may be expressed as follows:-

$$T(t) = P(t) - \left(P(t) - T_{t-1}\right)K \qquad \text{-(13)}$$

where - T represents the wire temperature, P is the sampled value of load current squared, and

$$K = e^{-\frac{sp}{\tau}}$$

where - *sp* is the sample period of the iterative cycle and τ is the time constant of the trip curve

The final operation in the procedure is to compare the wire temperature with the threshold value representing the square of the downstream wire rating. If the wire temperature ever exceeds this threshold then the software will issue a trip command.

7 TEST RESULTS FOR METHOD 2

The above algorithm was implemented on an 8 bit microcontroller test system which had the capability of interrupting power delivered to a load. This test system shown in block diagram form in figure 3.

Figure 3 - Schematic of Microcontroller Test System

The program constants were configured for a real specification trip curve (i.e. a 10 A type conforming to the MS3320 standard - see figure 1). The resultant plot of the current versus trip time output function generated by this I^2t algorithm is given in figure 4.

Figure 4 -Time Constant Method Results

From a comparison of the two curves it can be seen the digital implementation produces a current input versus time to trip function mirroring that of the MS3320 specification.

PERFORMANCE/ECONOMIC CONSIDERATIONS

Although the algorithm developed to provide true I^2t wire protection has proved both accurate and simple, there are however a number of considerations which should be taken into account in any real implementation. Since the algorithm is iteratively performing the function of equation (1), it is obvious the shorter the time duration between iterations the more continuous and accurate the operation. Similarly, a single digital I^2t implementation may be required to characterise the trip response of more than one protection device in real time (i.e. as in the case of a three phase supply). With such requirements, program execution time may be of significant importance to the performance of the device.

If an inexpensive microprocessor / micro-controller is used (as would almost certainly be the case if the product were to be economically viable) then the algorithm may pose efficiency problems in that it requires

two multiply operations, one for the squaring of the sampled input and the other for the multiplication by the exponential constant given in equation (13). Performing multiplication's using inexpensive microcontrollers is computationally intensive as they often lack the instruction support for this type of operation. If an 8 bit device is used (as was the case in the test system) the problem is further exacerbated in that an 8 bit A to D sampled input requires 16 bit operations internally. It is possible to improve performance somewhat by the inclusion of a look up table to perform the squaring function, but the exponential constant multiplication is more difficult since it will always be a number less than 1 and as such will require either floating point or fixed point arithmetic to carry out the calculation. Owing to the lack of dynamic range associated with this multiplication it is not possible to implement a look up table to perform the calculation. To this end the best execution time achieved on the test system for a single A to D sample iteration was 520μS.

8 METHOD 3 ANOTHER DIGITAL SOLUTION TO THE PROBLEM

Owing to the performance difficulties of the previous algorithm when implemented on small low cost microcontrollers, a second algorithm was developed which provided a considerably reduced execution time cycle. The algorithm differs from the Method 1 & 2 in the way it characterises the current versus time to trip curve.

Since the curve is simply a function of current and time, it is possible to characterise the curve by reading trip times for each value of current in the x axis and then dividing each time to trip by the sampling period. In this way a constant is generated for each value of current and this can then be stored as a look-up table indexed by the current value. All the trip algorithm need do is sample the load current, use the sampled value to index the corresponding constant and then add this constant to an accumulator. If the accumulator ever exceeds a threshold (given by the time to trip for the highest rated current value i.e. normally 1000% PU overload divided by program sample interval), then a trip command will be issued.

Although this method will generate a trip response in accordance with the specified current versus time to trip curve, the value in the accumulator represents a heating component only and as previously noted a cooling component is also required for correct operation of the protection device. Despite the fact the current versus time to trip curve contains no explicit information relating to this cooling component, it is however possible to make some important assumptions:

Figure 5 - Method 2 Parameter Extraction

At point A (see Figure 5) on the current versus time to trip curve, the protection device is in a state of equilibrium, that is, at the current value corresponding to point A, the energy into the device is equal to that of energy lost through conduction, convection and radiation.

Using this assumption it is possible to derive a cooling term (Ic^2) as a value of the square of the load current. Since heating is again a function of the square of the load current at the very high values of current over which the protection device is designed to operate (see Figure 5 point B) it can be assumed the effects of cooling are negligible.

Using these two assumptions it is possible to solve the problem on a computational engine which performs a numerical integration at a regular sampling time interval using the formulae -

$$\Delta T = \sum_{0}^{t} (Pin - Pout) \qquad \text{-(14)}$$

where ΔT is the temperature change of the downstream wire, t is the sampling period, Pin is the wire heating component, and $Pout$ is the wire cooling component.

As the number of samples increases and consequently $t \rightarrow \infty$, we have

$$\lim_{t \rightarrow \infty} \left(\sum_{0}^{t} (Pin - Pout) \right) = \int_{0}^{t} (Pin - Pout)\,dt \qquad \text{-(15)}$$

by the MacLaurin-Cauchy theorem. If the constant CV of equation (2) is equated to unity, the right hand side of (14) becomes equation (2). Thus these two equations (i.e. 2 & 14) are equivalent for an infinitely small sampling time.

Equation (15) can be translated into the following algorithm :-

$$Acc_n = Acc_{n-1} + Heating - Cooling \qquad \text{-(16)}$$

where Acc_n is a value representing the new temperature of the wire and Acc_{n-1} is a value representing the old temperature.

The routine will issue a trip command if ever the value of Acc_n exceeds a constant threshold (Acc_{max}). This

constant is a product of the square of the maximum load current over which the protection device is to operate $(Imax)^2$, the time to trip for that value of current ($Tmax$) and the sample interval and is thus given by:-

$$Acc_{max} = I\max^2 * \frac{T\max}{Sample\ Period} \qquad -(17)$$

and

wire heating is simply:

$$Load\ Current_n^2 \qquad -(18)$$

where n is the sample value
in addition,

$$Wire\ cooling = Ic^2 * \frac{Acc_{n-1}}{Acc_{max}} \qquad -(19)$$

9 TEST RESULTS FOR METHOD 3

The above algorithm was again implemented on the test system and the program constants configured for the same 10A MS3320 trip curve. The execution time achieved with this algorithm for a single A to D sample iteration was 35μS (including the 10μS A to D conversion time) showing a dramatic improvement over the previous algorithm.

The resultant current versus trip time function generated by this heating/cooling I^2t implementation model is shown in Figure 6.

Figure 6 - Heating Cooling Method Results

From a comparison of Figure 1 with Figure 6 it is seen that this digital implementation generates an output response mirroring that of the MS3320 current versus time to trip curve. It is also interesting to note that when the test results from this digital algorithm are compared with the test results of the thermal time

constant algorithm (see Figure 4) they produce almost identical results, showing that the results are a good practical indication of the theory.

10 DISCUSSION

It has been demonstrated the two digital methods described for generating an I^2t trip response develop near identical test results. The time constant algorithm of Method 2 has the advantage of low memory overhead at the expense of an increased execution time. The heating/cooling algorithm of method 3 is computationally more efficient, but this is gained at the expense of increased memory usage.

The tested accuracy of the trip response generated on the test system by both digital methods was demonstrated to deviate by less than 1.3% from the MS3320 mid-point value. This compares favourably with the large tolerance band displayed on the existing trip curves which define acceptable behaviour for electro-thermal devices. Inaccuracies in the digital solution were primarily attributable to the accuracy of the current to voltage measurement transducer and the precision of the A to D converter. Increased accuracy of the trip curve facilitates tighter co-ordination between protection devices in a power distribution system . This increases the likelihood that only the device nearest the fault will interrupt the supply of power. Likewise, depending on the inrush requirements of the load, it may also allow the current rating of certain power feeders in the system to be reduced, saving both space and cost.

Despite the fact the analogue solution could probably be made to work by selecting the correct components, the digital approach is likely to be 'cleaner' and easier to implement in a practical device The tested accuracy of the digitally generated trip curve was demonstrated not to be compromised by device temperature variations or the difficulties of accurately generating large time constants using passive components. The digital implementation may also claim an advantage in relation to size and flexibility, since only variables need change to characterise different I^2t curves. Indeed it has been demonstrated, the digital method may produce a trip response conforming to I^nt where *'n'* can be any index. This feature will allow device co-ordination under difficult circumstances e.g. an electrical load with an unusually large inrush requirement.

11 CONCLUSION

This paper has attempted to show that by using inexpensive digital technology it is possible to provide a solid state power controller with a true I^2t trip function mirroring that provided by a traditional fuse or

electro-thermal circuit breaker. Since both algorithms perform an integration on the input value of current, wire behaviour is modelled in both the heating and the cooling phase. The paper has also defined a number of techniques which can be used to characterise an existing trip curve, facilitating the matching of new solid state protection technology to older legacy systems based on electro-mechanical devices.

Although the paper has specifically targeted solid state controllers as the recipient of the digital I^2t generation technique, existing electro-mechanical contactors (i.e. a power interruption relay) can equally make use of this technology to accurately control their trip point. At present digitally controlled circuit breakers are restricted to relatively high end, high cost applications. Since the digital methods defined in this paper make no reliance on expensive or specialised hardware, the solution could feasibly form part of a practical unit to replace circuit breakers or fuses in the low cost sector of the market.

12 ACKNOWLEDGEMENTS

This research has been directly supported by Smiths Industries Ltd. The author would like to thank Dr David Elliott of Smiths Industries Corporate Research for his helpful comments and suggestions regarding details of digital method 3; Dr Stella Mills of the Cheltenham and Gloucester College of Higher Education and Dr Keith Rawlings of Smiths Industries Corporate Research for their valued contribution in reviewing this paper..

13 REFERENCES

1. Friedman, S.N.:'Solid State Power Controllers for the next generation'. IEEE National Aerospace and Electronics Conference 1992, Vol. 1, pp. 155-162.

2. Simon, J.J.: 'State of the art for solid state power controllers for aeronautical applications'. Fifth European Conference on Power Electronics and Applications, 1993, Vol. 8, pp. 121-126.

3. Meyer, G.J.: 'On the theory of fuses'. Munich 1906.

4. IEEE committee report. Computer representation of overcurrent relay characteristics. Transactions on Power Delivery, Vol. 4, No. 3, July 1989, pp. 1659-1667.

5. MS3320 Time Current Characteristic Specification Keuffel & Esser Co. Oct 1989.

6. Fidinger, J.A and Vincent, J.R.: 'Low voltage circuit breaker modernisation through solid state technology'. Industrial Applications Society 38th annual Petroleum and Chemical Industry Conference 1991 pp 193 - 197.

7. Urie, J.B.: 'Specifying a circuit breaker for your product'. Electrical Manufacturing May/June 1992 pp. 18-19

8. Balasubramanian, K.: 'Eprom based overcurrent relays', Proceedings of the 38th IEEE Holm Conference on Electrical Contacts 1992, pp 203-207.

9. Purkayastha, I and Savoie, P.: 'RMS digital trips offer increased accuracy and reliability advances in low voltage circuit breaker trip technology'. IEEE Transactions on Industrial Applications, 1990 Vol. 26. No. 1, pp 160-166.

10. Chowdhury, S.P. and Chowdhury, T, and Banerjee, S.: 'Software implementation of overcurrent relay characteristics for industrial power systems protection'. Modelling Measurements and control, A,AMSE Press Vol. 53, No 4 1993, pp. 41-4.

11. M.P. Murskyj, A.J. Alsammarae, Alternative methods of protecting power circuits. International Journal of Energy Systems, Vol. 12, No. 1, 1992.

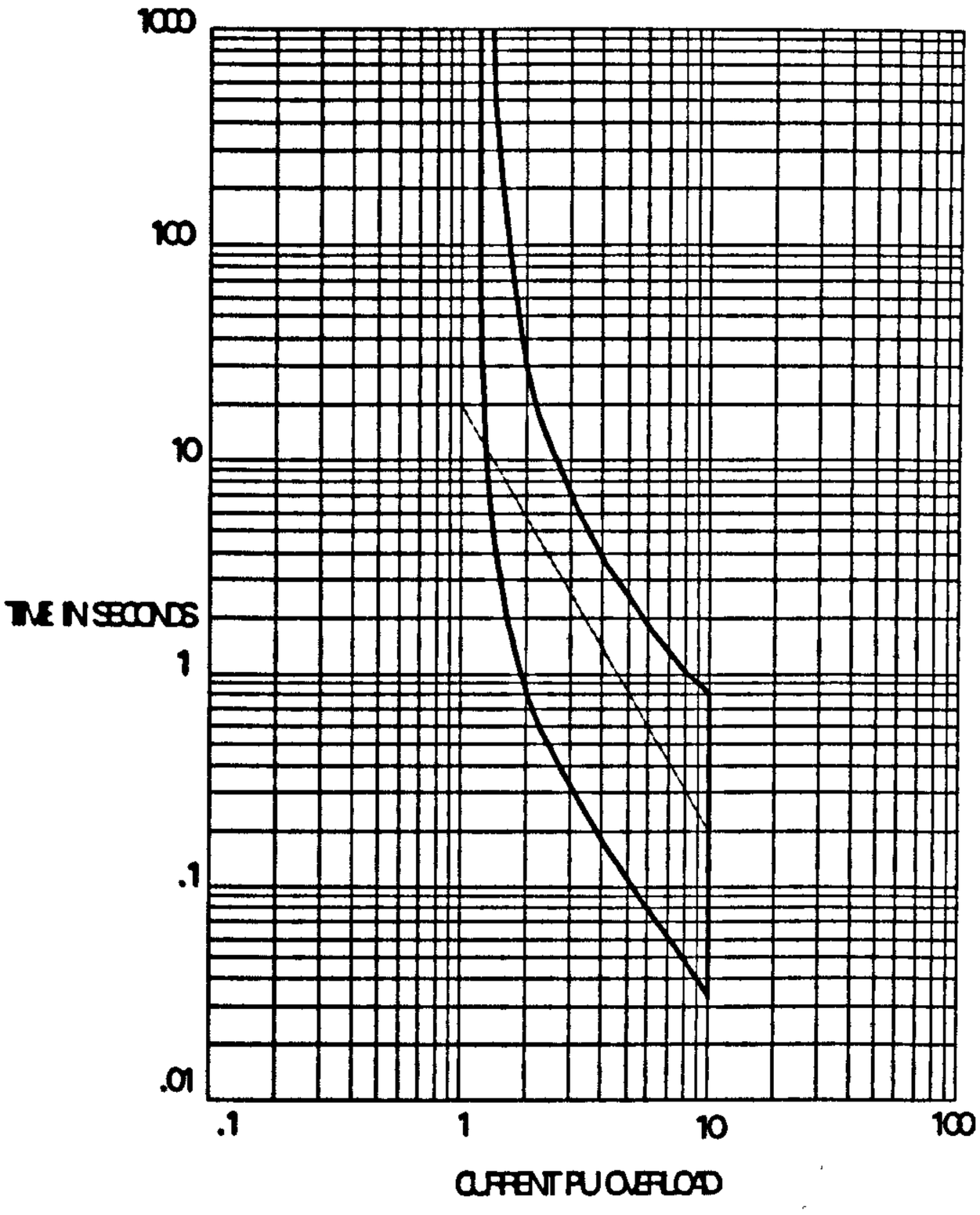


Figure 1 - MS3320 Current versus Time to Trip Curve

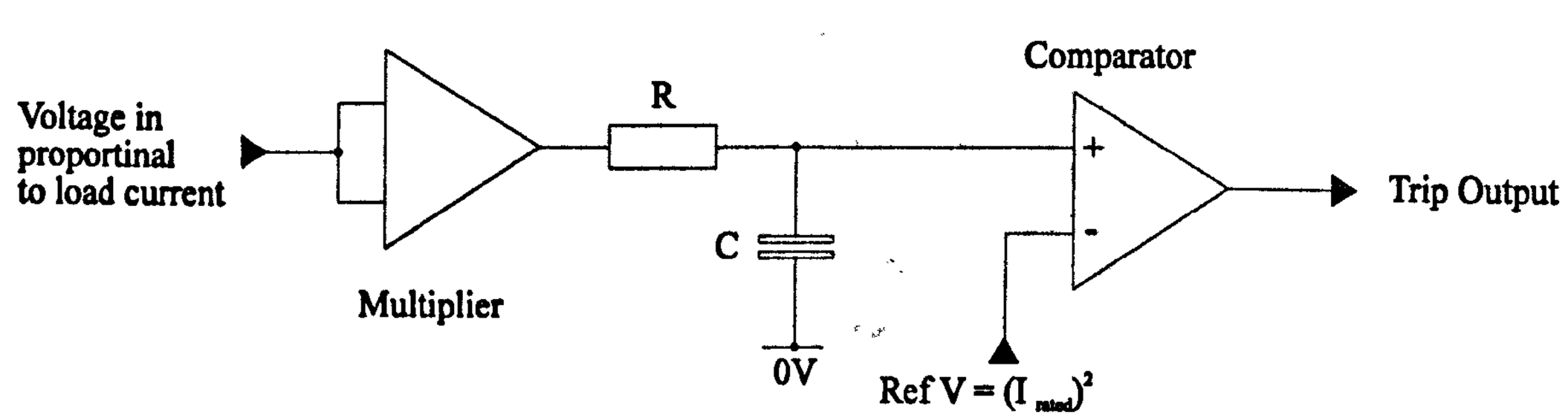
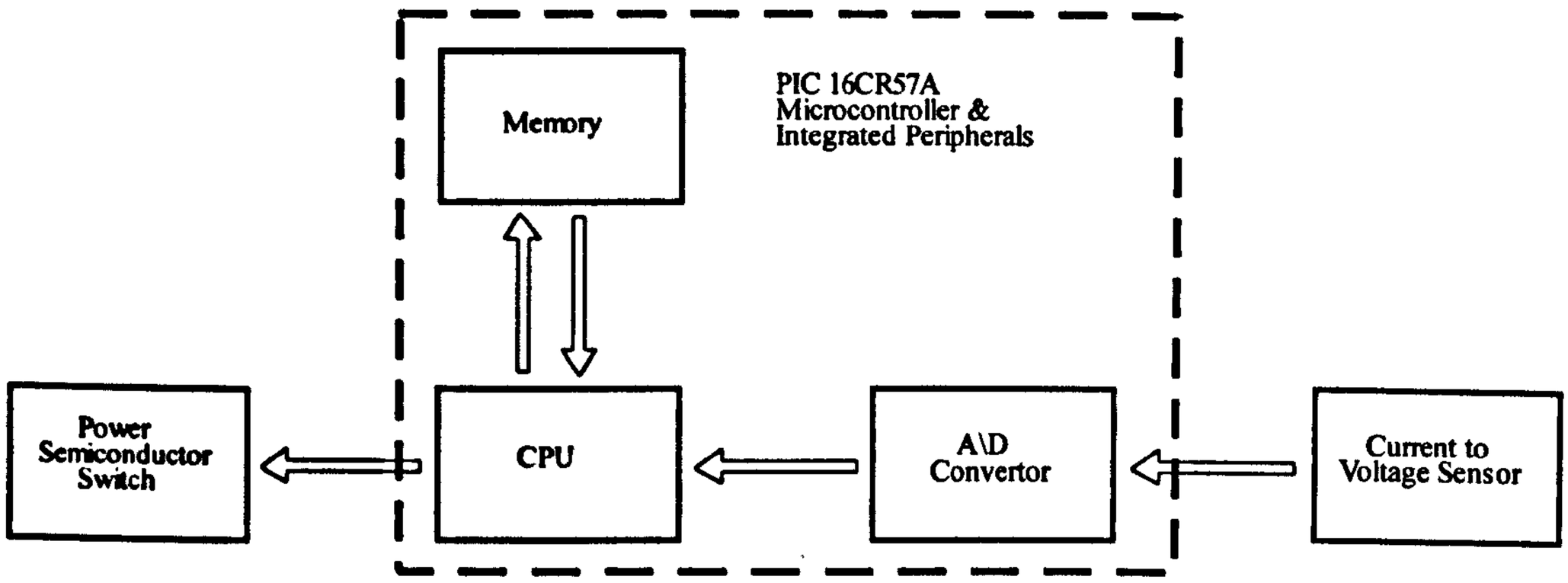


Figure 2 - Analogue I^2t Implementation



Note - Current to Voltage sensor = terminated current transformer for ac operation
= shunt resistor for DC operation

Figure 3 - Schematic of Test System

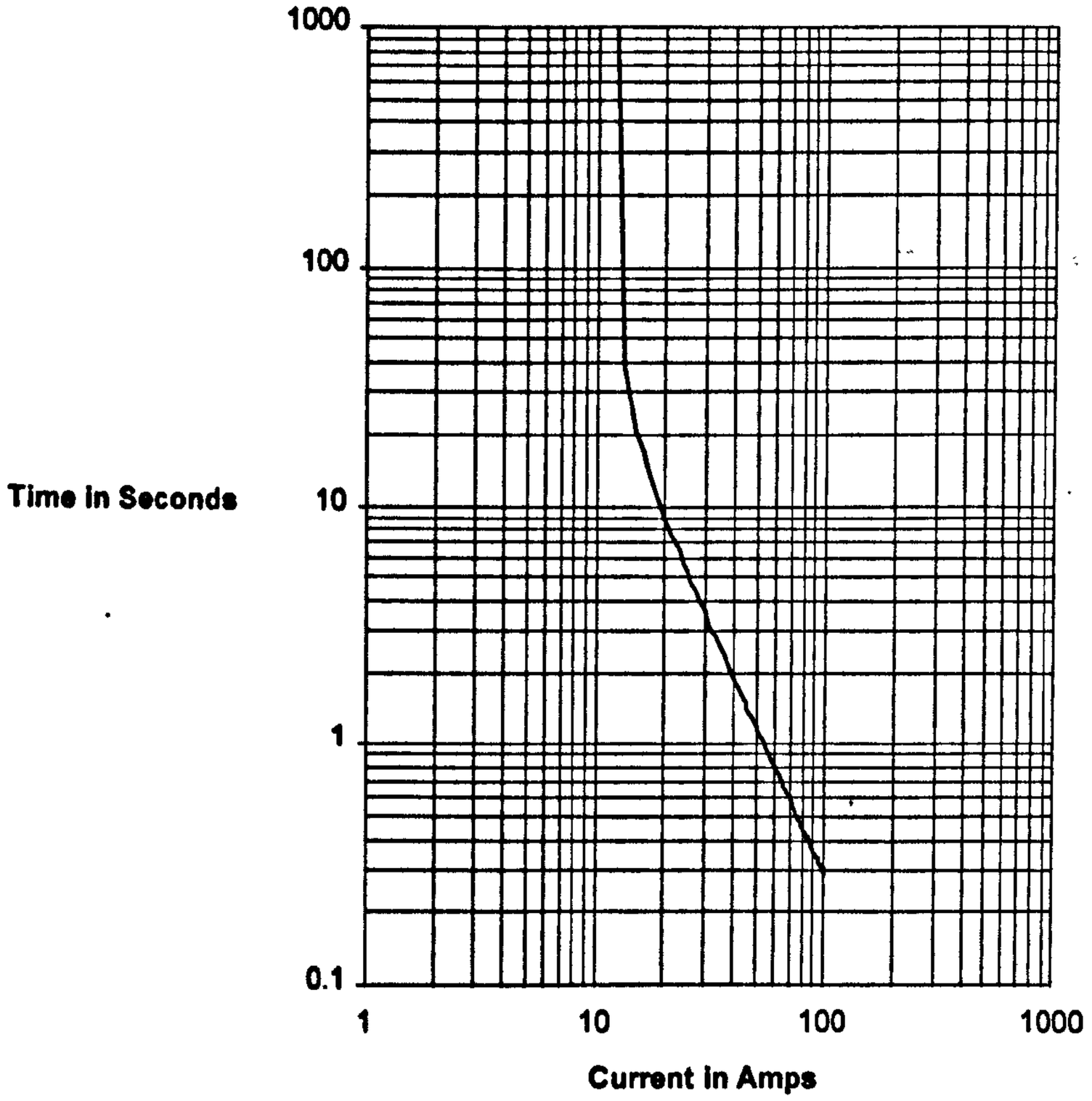


Figure 4 - Time Constant Method Results

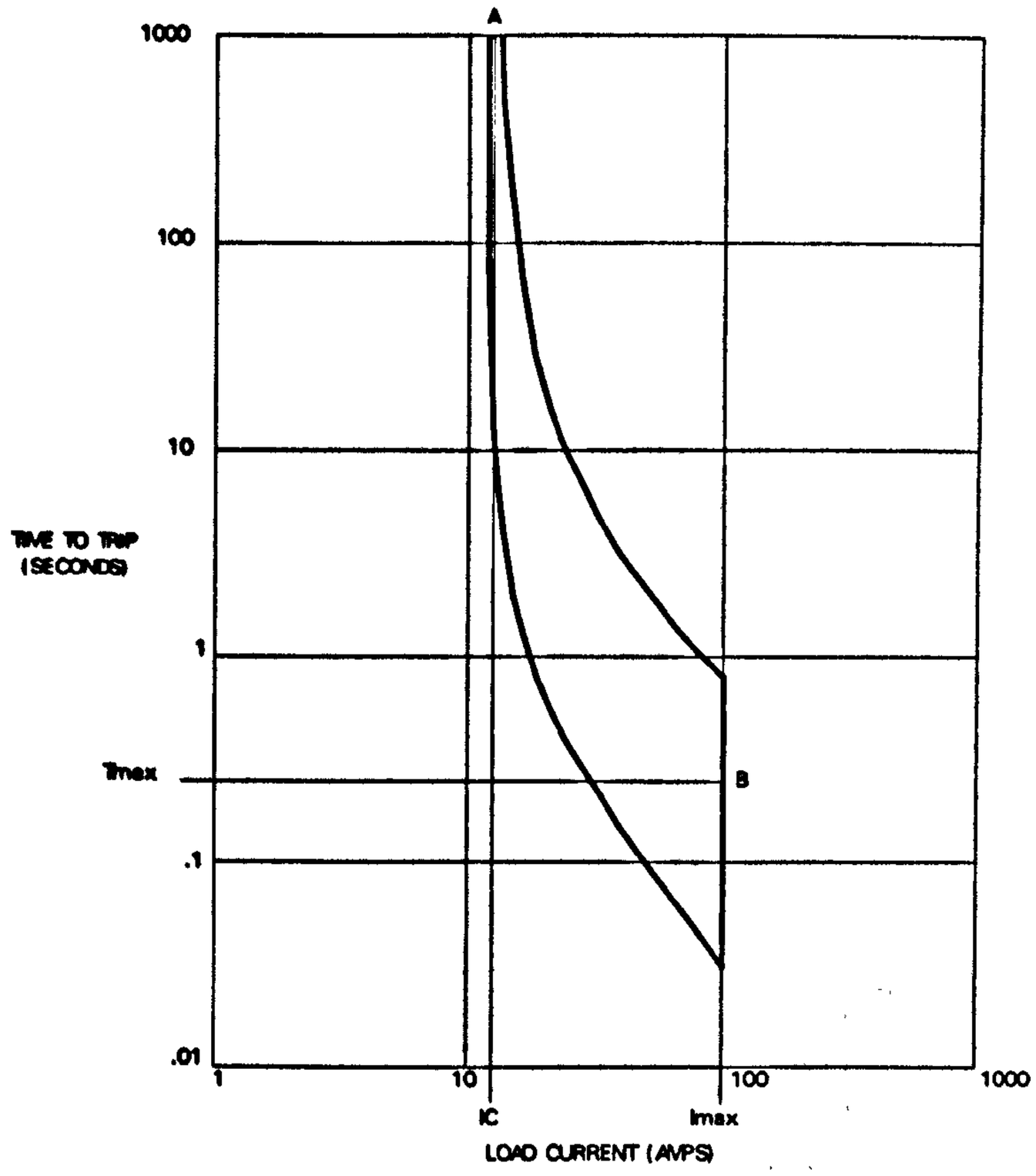


Figure 5 - Method 2 Parameter Extraction

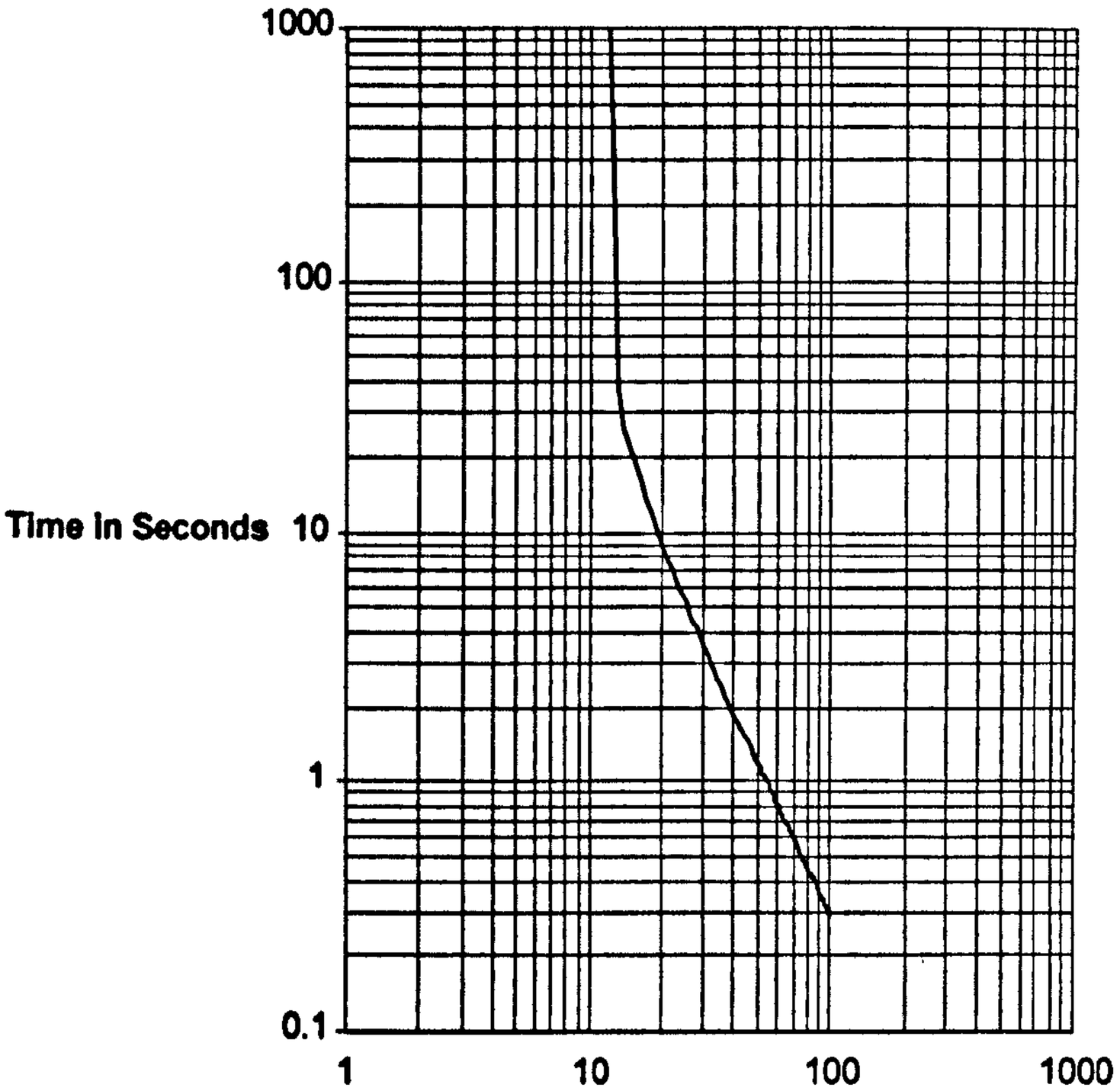
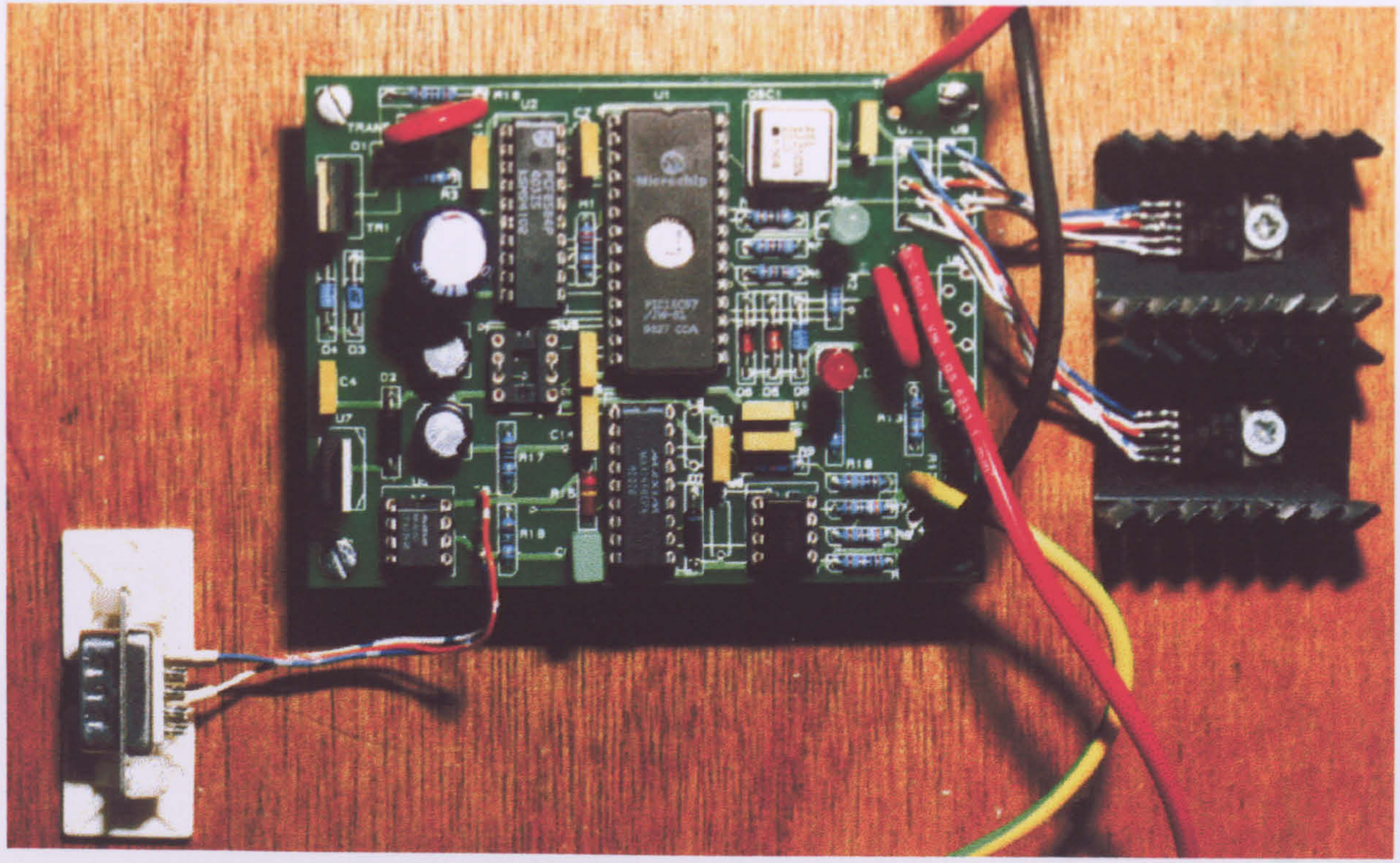


Figure 6 - Heating Cooling Method Results

Appendix 6:

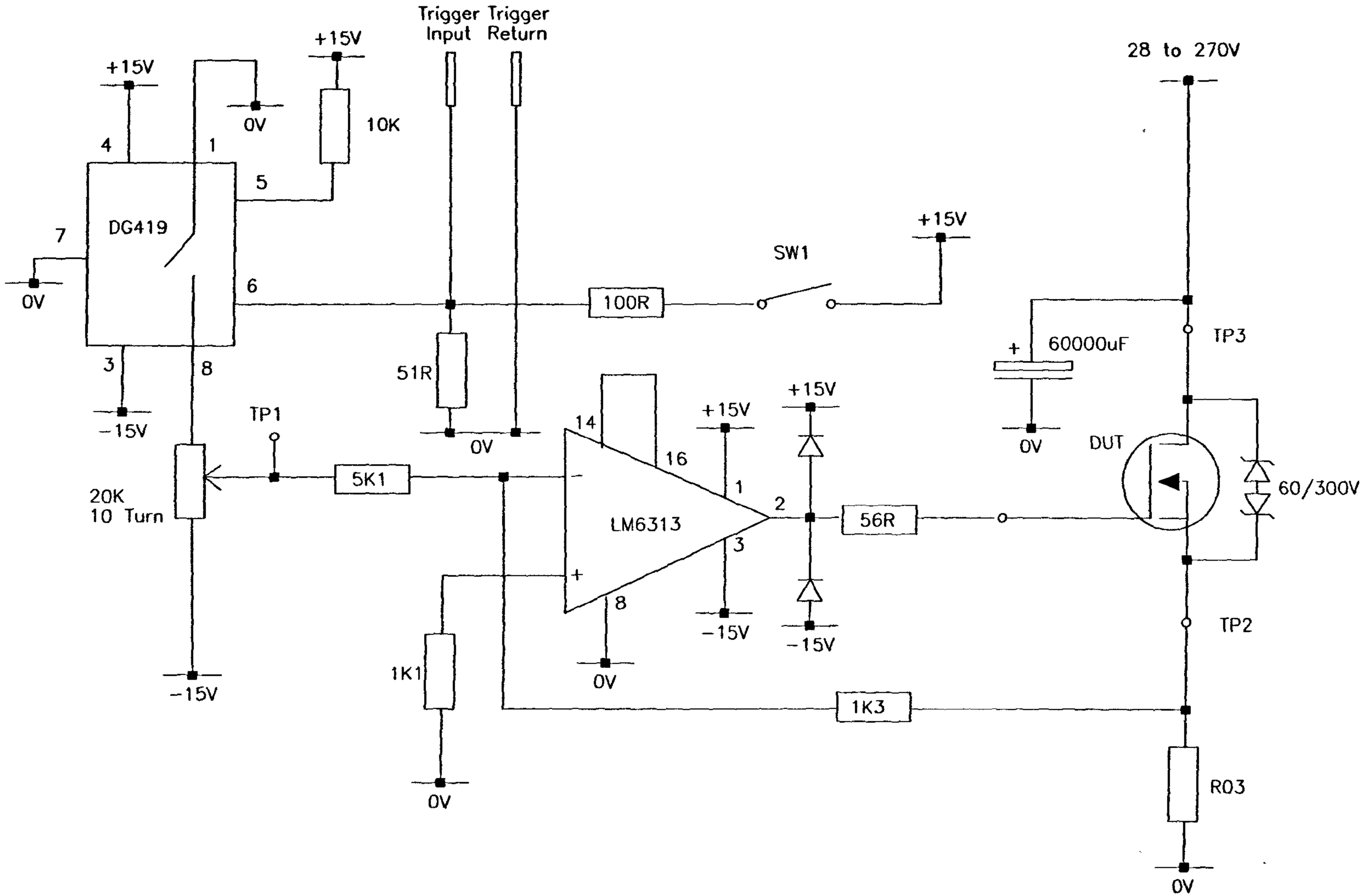
Photograph of I^2t Test Circuit



Photograph Showing the Circuit Used in I^2t Algorithm Evaluation Tests

Appendix 7:

Circuit Diagram of Test Circuit Developed For Infrared MOSFET Temperature Tests


Trigger Input
Trigger Return
+15V
+15V
0V
10K
4
1
5
DG419
7
0V
6
3
8
−15V
TP1
20K
10 Turn
−15V
5K1
51R
0V
14
16
1
2
3
LM6313
+15V
+15V
−15V
−15V
8
0V
1K1
0V
100R
SW1
+15V
1K3
28 to 270V
+
60000uF
0V
TP3
DUT
60/300V
TP2
56R
R03
0V

Appendix 8:

Example of a Thermal Simulator Input File for an IRF044 Power MOSFET

Power device IRF044
PROGRAM PROCEDURES AND GLOBAL VARIABLES
Mode= n
Number of levels = 6
Dissipating layer = 2
Beta= 0.935
Average final residue= 0.10E-04
Ambient temperature= 0.0
Base temperature= 54.0
Output bfile= y Read bfile to start= n
Compute and add surface integral error= y
Maximum number of iterations= 700
DIMENSION SPECIFICATIONS MATERIALS AND CONDUCTIVITIES
Chip dimension is 3265. by 3265. microns
Grid in X direction
Entry 1 Number of elements= 10 Spacing = 316.5000
Entry 2 Number of elements= 1 Spacing = 100.0000
Grid Y direction
Entry 1 Number of elements= 10 Spacing = 316.5000
Entry 2 Number of elements= 1 Spacing = 100.0000

Layer 1 specified below, Dimensions- 12 by 12
Layer 2 Is Silicon
Thickness= 15.0000 microns Layer dimension= 6 Pitch= 3.00
Layer 3 Is Silicon
Thickness= 35.0000 microns Layer dimension= 5 Pitch= 8.75
Layer 4 Is Silicon
Thickness= 120.0000 microns Layer dimension= 5 Pitch= 30.00
Layer 5 Is Silicon
Thickness= 220.0000 microns Layer dimension= 4 Pitch= 73.33
Layer 6 Constant conductivity
Thickness= 40.0000 microns Layer dimension= 4 Pitch= 13.33
Thermal conductivity= 36.50Wm/C
Chip thickness is 430.00um Not including metal

SOURCES
Number of sources= 1
Source 1
X1Y1Z1= 0.00 0.00 1.00 X2Y2Z2=3165.003165.00 8.30
Power input= 125.0000

Power density 1 = 0.17E+13
Total power input=125.000000 watts

SINKS
No bond wires
SURFACE FEATURES
Top layer spacing from the top in microns
2.000 1.000 1.000

Material type = 1
Material conductivity = 237.00 wm/C
Material spec type = c

Surface layer is dimensioned 3 vertically

Coordinates for Layer 1
Top layer 1 to 3
Feature No= 1 X 0.00 to 3165.00 Y 0.00 to 3165.00 type= 1
VIAS
No vias
CHIP BASE
Base details
Base X = 4250. Y = 6000. microns
Chip is 0.0 microns from base X edge
Chip is 0.0 microns from base Y edge
Base grid in X direction
Base entry 1 Number of elements= 10 Spacing = 98.5000
Base grid in Y direction
Base entry 1 Number of elements= 10 Spacing = 273.5000
Base dimensions are 22 by 22
Number of base layers= 3

Layer 7 Constant conductivity
Thickness= 1000.0000 microns Layer dimension= 5 Pitch= 250.00
Thermal conductivity= 400.00Wm/C

Layer 8 Constant conductivity
Thickness= 1600.0000 microns Layer dimension= 4 Pitch= 533.33
Thermal conductivity= 400.00Wm/C

Layer 9 Constant conductivity
Thickness= 150.0000 microns Layer dimension= 4 Pitch= 50.00
Thermal conductivity= 0.50Wm/C

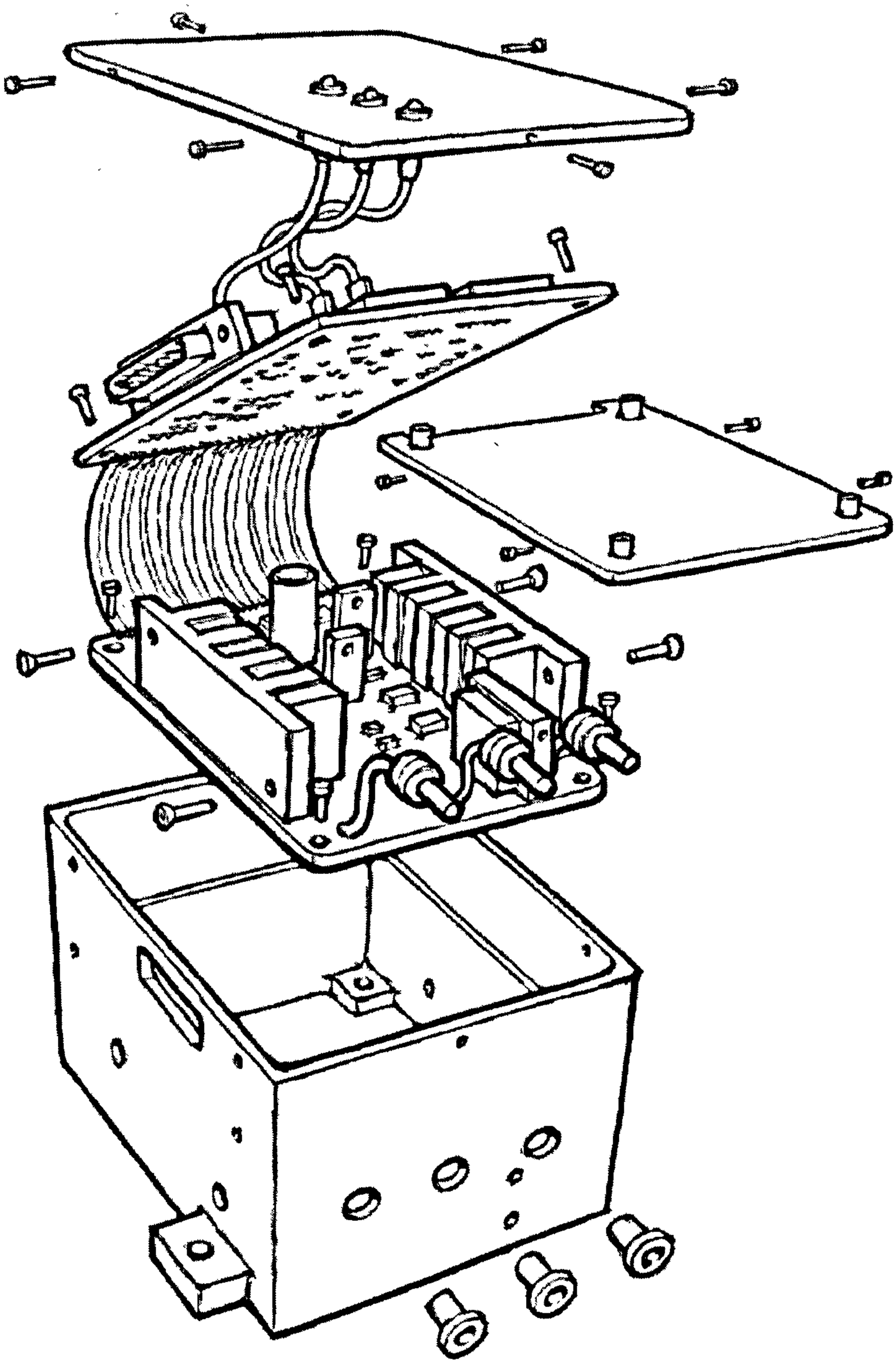
Base thickness is 2750.000um
CHIP OUTPUT PLANE
Output level= 2 plane= 1

-----Read Complete----

Total Pad Storage= 19289 words
Bfile storage= 10180 words
Integer storage= 432
Storage for opad= 3888

Appendix 9:

Exploded View Showing SSPC Construction



SSPC Mechanical Construction

Appendix 10:

Digital Solid State Power Controller Circuit Diagrams

28V DC
V_RAIL_SENSE
7K5 R3
1K1 R2
0V
(14) 1K4 R8
4V7 ZEN2
4816P-T01
4609X-470
47R R18
(12) FET1_I_SENSE 4K7 R9
(11) FET2_I_SENSE 4K7
(10) FET3_I_SENSE 4K7
(9) FET4_I_SENSE 4K7
(5) FET5_I_SENSE 4K7
(6) FET6_I_SENSE 4K7
(7) FET7_I_SENSE 4K7
(8) FET8_I_SENSE 4K7
47R
C9 0.1uf
10R R12
F1 F2 F3 F4 F5 F6 F7 F8
d g s
V33ZA5 Varistor
VAR1
D1 UF5404
IRFP054 (*8)
276
R005 R29 R28 R27 R26 R25 R24 R23 R22
(13) I_RAIL_SENSE
ZEN1 4V7
C6 10nf C21 10nf
0V
1K4 R1
10pf C11
R14 910R
6K2 R17
+15V
100uF C2
0V
R7 22K
I_CONTROL
(4) 22K R6
V_REF
(3) 24K R4
1K5 R5
U2 TL072-a
U1 AD847JR
+vs -vs
R11 100R
U3 V+ EL2008CN V-
10BQ040 D5
10BQ040 D3
D2 BAS16
T1 FMM618
R8 390R
Not fitted R31
C4 0.1uF
R15 51K
U2 TL072-b
2K R19
R16 2K
R001 R21
28V SWITCHED OUTPUT
0V (internal ref only)
C10 10pf
820R R13
100uF C1
-15V
C5 0.1uF
R30 51K
UF5404 D9
R20 10K
28V DC (RET)

SSPC 28V DC
Output Block.
MODEL MARK 2
K.P.Thomas 14.3.95

SK_1

CAN VCC (+5V) 26

CAN_H 8

CAN_L 9

CAN GND (0V) 18

DISCRETE_ON 14

0V DISCRETE 5

+28V ESSENTIAL 20

0V ESSENTIAL 19

5V_OUT 24 25

SPROM_CLK 12

SPROM_IN 3

RESET_2 1

RESET_1 10

RS_232_TXD 6

RS_232_RXD 7

TEST_DISCRETE_OUT 13

BOOTSTRAP_SELECT 4

0V_REF 17

CAN_TXD

CAN_RXD

ISOLATED_DISCRETE_ON

RESET

RS232_TXD

RS232_RXD

TEST_DISCRETE_OUT

BOOTSTRAP_SELECT

U4 HCPL0600

U5 HCPL0201

U6 HCPL0201

U7 SI9200DY

U10 MAX 202

U11 74ACT04M

R15 510R

R16 1K5

R25 1K5

R26 0R

R27 0R

R30 1K

R31 30K

R32 0R

R33 2K

R34 10K

R35 Not fitted

R9 20K

R13 20K

C19 0.1uF

C20 0.1uF

C21 0.1uF

C22 0.1uF

C23 0.1uF

C24 0.1uF

C25 0.1uF

C26 100uF

C27 0.1uF

C28 0.1uF

C29 0.1uF

C36 0.1uF

C42 0.1uF

Not fitted 3K

D7 BAT54A

D8 BAT54A

D9 BAT54A

D10 BAT54C

D11 BAT54C

D12 BAT54C

D16 BAR43S

T1 FMM618

JP1

JP2

JPX

120R

277

SSPC 28V DC
Interface Block.
Model Mark 2

K.P.Thomas 14.3.95

PINS_VCC 17,46,56,72,82,93,109,126,136,144
PINS_VSS 18,45,55,71,83,94,110,127,139,143

+5V
10uF C6 0V
C39 0.1uF 0V
142 NMI
PINS_VCC
VCC

8 bit = JP8 & JP10
16 bit = JP7 & JP9

C43 to C51 0.1uF

+5V C40 0.1uF 0V
+5V C41 0.1uF 0V

D7 D6 D15 D8
10K 10K 10K 10K
R2 R1 R4 R3
JP4 3 6 5
+5V
0V

R11 51R
(3) V_REF
C9 0.1uF
4.1V D3
0V

117 D15
116 D14
115 D13
114 D12
113 D11
112 D10
111 D9
108 D8
107 D7
106 D6
105 D5
104 D4
103 D3
102 D2
101 D1
100 D0
37 VAREF
38 VAGND

INT_V_THRES 20 POUT1
OVERLOAD_INT 57 EX01N
ISOLATED_DISCRETE_ON 52 P2.5
TEST_DISCRETE_OUT 53 P2.6
5V_LEVEL_SENSE 43 AN14
INT_V_THRES_SENSE 42 AN13
(8) FET8_I_SENSE 40 AN11
(7) FET7_I_SENSE 39 AN10
(6) FET6_I_SENSE 36 AN9
(5) FET5_I_SENSE 35 AN8
(9) FET4_I_SENSE 34 AN7
(10) FET3_I_SENSE 33 AN6
(11) FET2_I_SENSE 32 AN5
(12) FET1_I_SENSE 31 AN4
(13) I_RAIL_SENSE 28 AN1
(14) V_RAIL_SENSE 27 AN0

138 XTAL1
137 XTAL2
20MHz XTAL
22pF C1 0V
22pF C2 0V
RESET
R29 0R
RSTIN 140
C3 10uF 0V
VSS PINS_VSS
EA 99 0V

C167 CR
U1

A17 85
A16 135
A15 134
A14 133
A13 132
A12 131
A11 130
A10 129
A9 128
A8 125
A7 124
A6 123
A5 122
A4 121
A3 120
A2 119
A1 118
A0
CS0 1
WRL 96
WRH 79
RD 95

JP7
JP8
JP9
JP10

AM29F010 U2
32
2 A16
3 A15
29 A14
28 A13
4 A12
25 A11
23 A10
26 A9
27 A8
5 A7
6 A6
7 A5
8 A4
9 A3
10 A2
11 A1
12 A0
22 CS0
D15 21
D14 20
D13 19
D12 18
D11 17
D10 15
D9 14
D8 13
GND 16 0V
WRH 31
RD 24

AM29F010 U3
32
2 A16
3 A15
29 A14
28 A13
4 A12
25 A11
23 A10
26 A9
27 A8
5 A7
6 A6
7 A5
8 A4
9 A3
10 A2
11 A1
12 A0
22 CS0
D7 21
D6 20
D5 19
D4 18
D3 17
D2 15
D1 14
D0 13
D4
10K R14
GND 16 0V
WRL 31
RD 24

CAN_TxD 91 CAN_TXD
CAN_RxD 90 CAN_RXD
TXD0 77 RS232_TXD
RXD0 78 RS232_RXD
P2.4 51 S_PROM_CLK
P2.3 50 S_PROM_IN

P3.4-7 69,70,73,74 D6 ON (Green) R10 1K2 +5V
P3.0-3 65,66,67,68 FAULT (Red) D5 1K2 R24
R8 10K
P2.0 47 PWR_OUT_ENBL (Hi=Off, Lo=On)

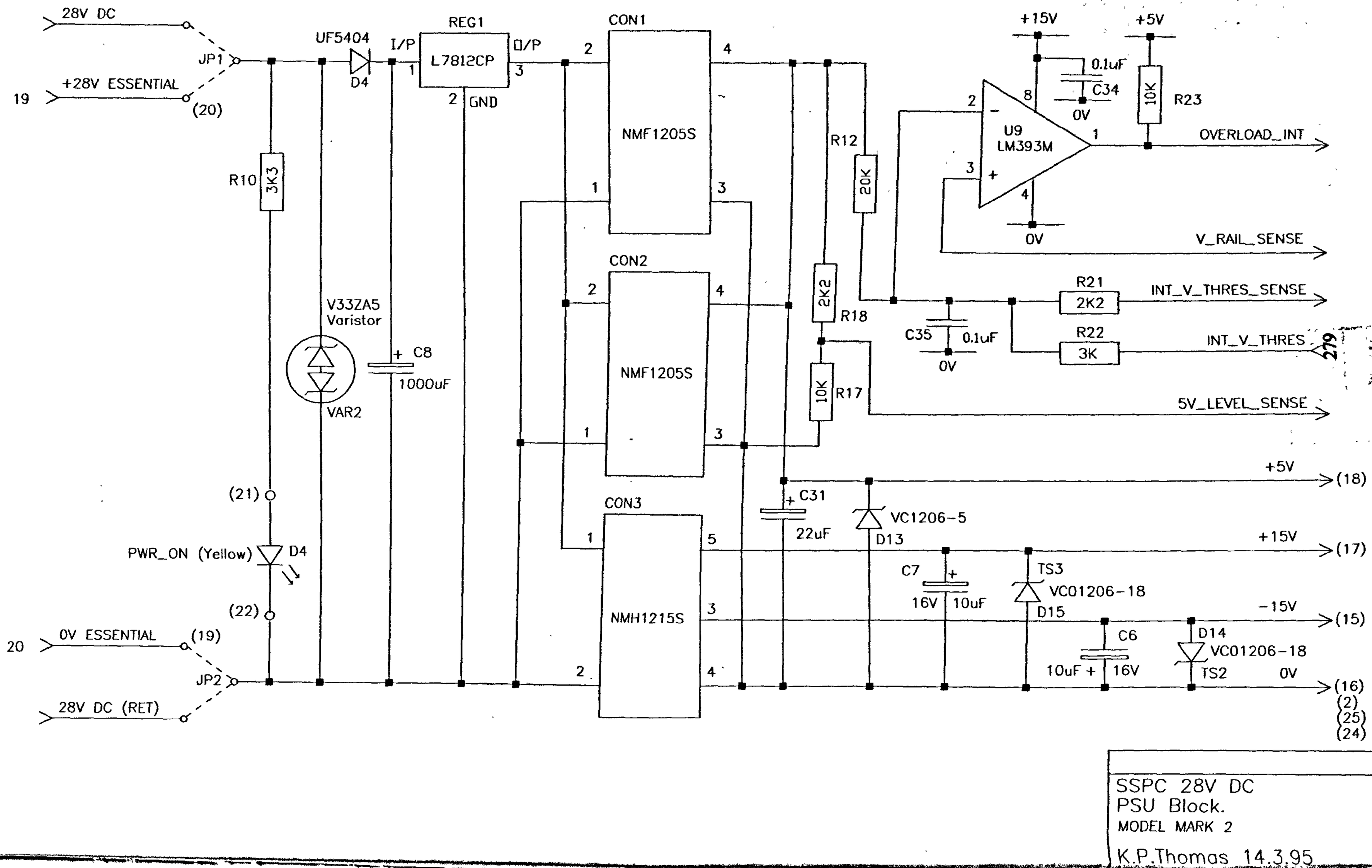
+5V +15V
D2 BAS16
0.1uF C38 0V
12 VL
13 V+
1 IN1
16 IN2
15 D2
2 D1
11 S3
D3 10
S1 3
S2 14
IN3 9
V- 4
GND 5
IN4 8
DG413 U8
I_CONTROL (4)
10pF C7 0V
BOOTSTRAP_SELECT (Hi=Normal, Lo=Bootstrap)

AN12 41
R7 10K
POUT0 19
R5 1K
AN3 30
+5V
R6 20K
V_REF
10uF C30
AN2 29
0.1uF C37 0V
BAS16 D1
-15V

(1) 510R R19
(23) 510R R20
Heatsink Thermistors
C11 0.1uF 0V
C10 0.1uF 0V
0V

278

SSPC 28V DC
Processor Block.
MODEL MARK 2
K.P.Thomas 14.3.95



SSPC 28V DC
PSU Block.
MODEL MARK 2

K.P.Thomas 14.3.95